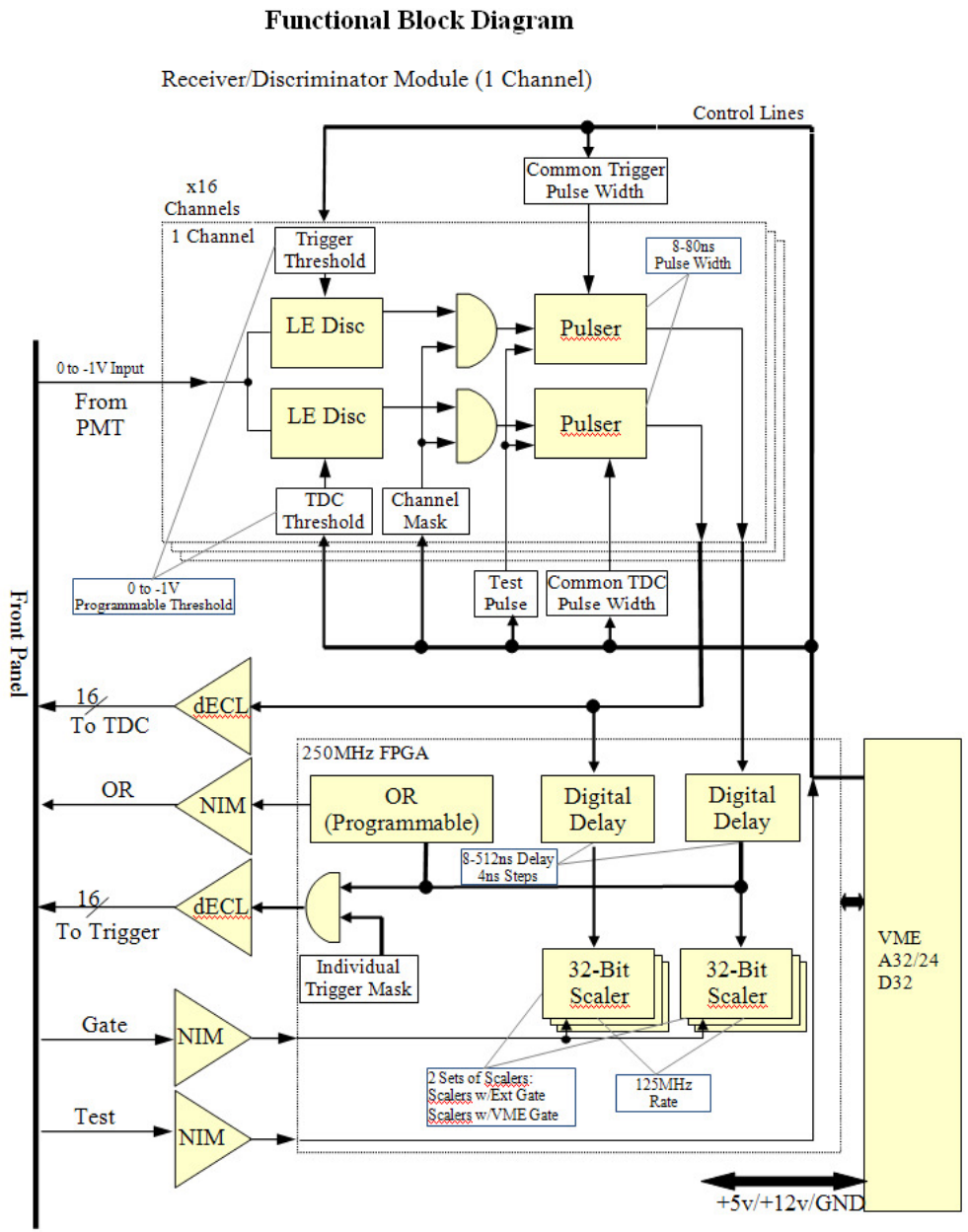
Hall B 12GeV Discriminator Module Design



Main Features:

- 16 Channel, Dual Threshold, VME (0 to -1v in 0.25mV steps)
- Differential ECL 'TDC' Output
- Differential ECL 'Trigger' Output
- Programmable Delay on Trigger Output (4ns Resolution)
- Internal & External Gated 125MHz Scalers both thresholds
- Programmable NIM input/output (i.e. OR output, TEST input)
- 100MHz Rate (w/8ns Pulse Width) => 10ns Pulse Pair Resolution

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Main Specifications

General	
Power consumption (typ)	+12V, 600mA; -12V, 0A; +5V, 6.0A
Fuses	+12V, 2.0A; -12V, 0A; +5V, 10.0A
Dimensions	6U VME, Single-wide; 160mm card depth
Front Panel I/O connectors	Input Signals: 16 LEMO Gate Input: 1 LEMO Test Input: 1 LEMO Dual dECL Output: 2x 34-pin Header OR Output 1 LEMO
On-board connectors	JTAG: 2x7pin 2MM pitch (Xilinx Platform USB)
LEDs	Green: VME Activity Yellow: Discriminator OR Red: FPGA Heartbeat
Analog Inputs	From PhotoMultiplier Tubes or coaxial detector signals
Channels	16
Signal level	± 1.5V, DC-Coupled, diode-clamped
Termination	50-Ohm
Gate Inputs	Gates scalers
Channels	1
Signal Level	NIM
OR Output	1
Signal Level	NIM
Discriminator Channels	
Dual Threshold Control	0V → -1V threshold (1 threshold per TDC and Trigger output, 32 total)
Pulser type	**Non-updating**
Pulser control	TBD control voltage = 8nS → 80nS pulse width
Channel-to-Channel crosstalk	<1mV for rise time ≥ 1nS & Vin = -200mV (46dB ch-ch Isolation)
Discriminator hysteresis	5mV
Discriminator noise band	<±2mV (no adjacent modules)
Pulser dead-time	<2nS
Discriminator Offset Error	<±3mV max, <±1mV typ.
Maximum Rate	100MHz (10ns double pulse resolution w/8ns pulse width setting)
dECL Outputs	
Channels	Dual 16 channel output
Connector	34-pin header in LeCroy ECL format.
1st group of 16	Fast output from discriminator Common programmable width 10ns – 100ns Programmable MASK register: - Default: Enable
2nd group of 16	Common programmable width 4ns – 100ns Programmable delay 4ns – 500ns Programmable MASK register - Default: Enable
Individual Discriminator Control	
DAC	12-Bit; Set to zero by logic after reset. 0.25mV Step
Threshold control	DAC zero-scale = 0V, full-scale = -1V
Pulse width control	TBD zero-scale = MIN = 10ns, full-scale = 100nS
Minimum pulse width	10nS with DAC setting of ?mV
Digital Delay	
Delay step size	4nS, VME controlled
Delay range	0nS → 500nS
Uncertainty	4ns (250MHz Clock Jitter)
Maximum effective rate	250MHz
Delay from discriminator input to	
Digital delay input:	TBD
Scaler input:	TBD with delay setting = 0
Delay from Gate input to scaler logic	TBD
Scalers	
Quantity	1 per discriminator channel (32 total)
Width	32-bit
Input source	Digital delay circuit
Gating	Selectable: Front-panel gate input or VME controlled gate enable/disable
Maximum rate	125Mhz
Readout dead-time	None
Control	VME latch, read, clear, scaler overflow status
VME Interface	
Compliance	A32/D64, D32 only; D16/D08/unaligned not supported
Registers	TBD
Address space used	TBD
Misc.	
Voltage monitor	No
EEPROM	Stores configuration parameters (> 1kbyte)
Firmware Upgradable	Yes – via VME

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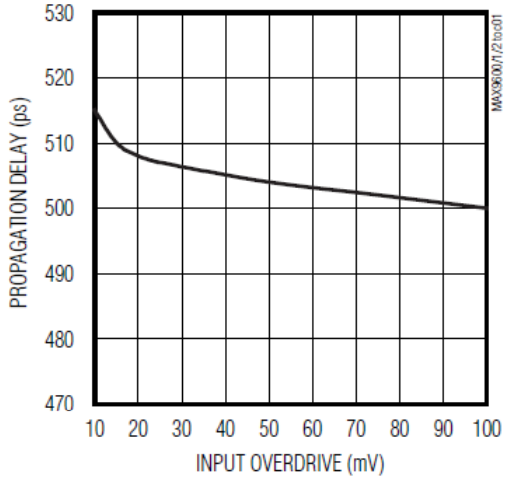
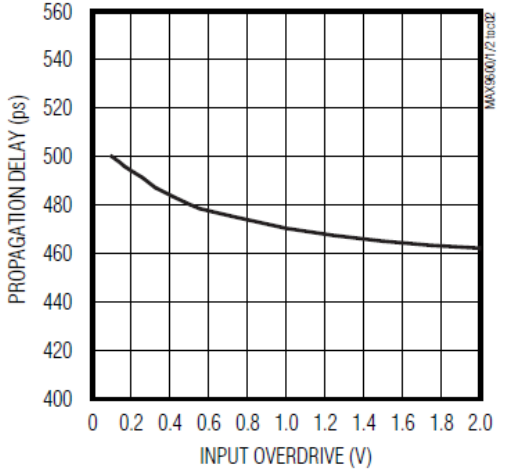
Comparator Dispersion Characteristics (does not include discriminator output stage dispersion)

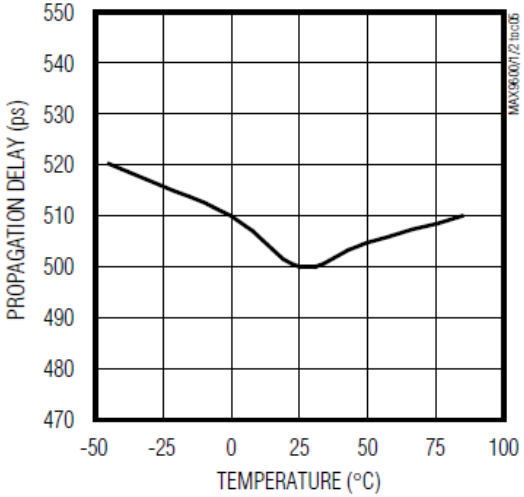
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{OD} = 10mV TO 100mV)



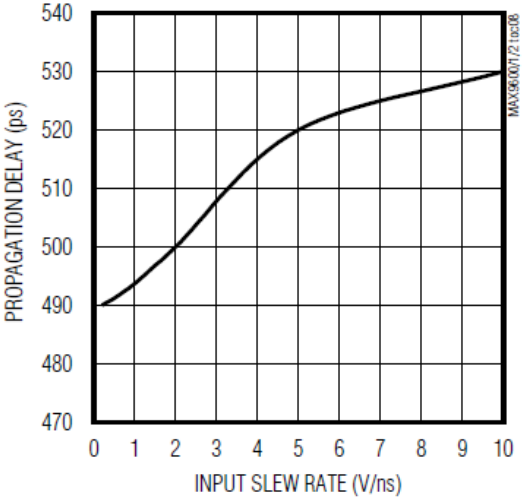
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{OD} = 0.1V TO 2V)



PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. INPUT SLEW RATE



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Current Layout Status