12GeV Trigger meeting notes:

26-October-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, B. Moffit

19-October-2012: Meeting cancelled

12-October-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, Beni Z. H. Dong, N. Nganga, B. Moffit

5-Oct-2012: Cancelled (Hall D Collaboration Meeting)

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0. Trigger/Clock/Sync – TI/TD

26-Oct-2012

→Exact delivery schedule with quantities not disclosed by CEM. The contract lists 20 weeks from acceptance date.
→William has reduced the overall latency to 490ns by adjustments to the receiver.
→Updated firmware for TI-D and TS has been released and Bryan is working on updating/creating the new CODA library.
→Pre-production boards have a slightly different pin out from the production versions. 10 TI production boards have been received, and 5 TD production boards have been received. William is distributing these production boards to the hall groups.

12 Oct-2012

→Deliveries of next batch of production boards unknown. Will receive schedule today.
→Repaired board has passed acceptance testing.
→William distributed a message regarding trigger latency measurements and there have been several discussions:

> The minimum TS to TI latency using the 62.5MHz trigger 'link' is rather long and is approximately 570ns. If the internal logic operates on a 125MHz clock this latency period can be reduced. Fiber distribution will add to this latency delay, and in the end the minimum requirement is 3.5us to be sure that timing hits are not lost for the F1TDC board.

→Changes to the TI-TD firmware is close to complete. Testing activities to begin soon after the firmware revision is ready.

1. *SUB-SYSTEM PROCESSOR (SSP)*

26-OCT-2012

-->Files have been updated on the M:drive for review. Only a few minor details still in flux, but folks should have a critical review. These are the production files and the goal is to have the files to Zentech by the week of 5-Nov-2012.
→Front panel and other peripheral items will be completed soon.
→Acceptance testing firmware/software procedure is in good shape and time for development while 1st article is under assembly.

12-Oct-2012

→An internal review of the fabrication data is imminent. Ben will continue to verify the new layout and set up a meeting time.
→Front panel and other peripheral work continues.

5-Oct-2012

→90% routed and the manufacturing files will be reviewed by several folks.

→Zentech has ordered the parts
→Still on schedule for sending files. 1st article due 8weeks after files and parts received.
→Acceptance testing code etc needs to be completed. Re-use of many routines from original SSP work can be used.

2. CUSTOMERS

26-OCT-2012
→CPU order has been evaluated and decision for initial purchase has been made. The initial purchase is for sixteen (16) units. Larger order for the Hall groups will be later in the year.

12-Oct-2012
→Full crate testing activities are imminent and FADC250 production boards will be here soon. Will need to re-use a CPU and CTP to complete the crate test.
→CPU production order is in the process of receiving evaluation models.

3. "B" Switch - Signal Distribution Module (SD)

26-Oct-2012
→Open development: Firmware iterations like SD→TI link, 16 bit "Logic" unit to handle the Trig_Out signals. (65K memory LUT)
→Three production boards remain at CEM for rework/repair issues. Once these are received, they will be tested and delivered to Hall group.

12-Oct-2012
→112/115 have been tested and passed.
→Distributed 58/60 to Hall D
→3 have been sent to CEM for rework/repair

4. System Diagrams/Fiber Optics

26-Oct-2012
→Prepare PR for Hall B and D order of patch cables and patch panel hardware. Trunk lines will need to be a separate order because exact lengths are not known at this time.

12-Oct-2012
→No update. A recent walk through of Hall D shows virtually zero cable trays or equipment racks. Trunk cable order will be dependent on the accurate lengths from the trigger racks to the various detector readout racks.

5. Global Trigger & Trigger Distribution Testing

26-OCT-2012
-->SSP→GTP backplane interface testing is progressing @5Gb/s. 4 lane streaming mode on the backplane, and the fiber interface is full blown 4 lane @2.5Gb/s which could be extended to 3.125Gb/s for show.

12-Oct-2012
→SSP->GTP testing is going well. The next step is to integrate the GTP output (all 32 bits) to the TS-SD-TD crate. Run at full trigger rate, use adjustable delay (processing time) in GTP and then ultimately connect to the front end crate to measure FULL system latency.

28-Sept-2012
-->Another VXS crate has been installed in EEL109. This will be used in the Global Trigger testing.
→Still need to locate a CPU and TI.
→Ultimate goal is to measure and record the final latency from the GTP → TS → TD →TI

20-JAN-2012 (Keep this date to reference full DAq crate procedure)

3-June-2011
→***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

26-OCT2012
→New CTP RFQ has been released for company bids (2-Nov-2012). The vendors have 2 weeks to deliver new quotes.
→Jeff and Hai have been busy with the routing strategies and the latest results look promising and the board is almost fully routed. Final route and close scrutiny of manufacturing files will be forthcoming.
→Automated test station procedure and firmware/software for the CTP-V2 acceptance testing is progressing nicely. Are there any other test support boards needed for this test procedure?

12-Oct-2012
→The production order for Hall D CTP was cancelled by the vendor. The new RFQ will be posted soon and there are no changes to the specification or BOM.
➔ Board routing is progressing and with the new bid process we have gained a few weeks of routing and verification time.
➔ Hai is very close to completion with the CTP automated acceptance test procedure.

28-Sept-2012
-->A week away from full time routing on the CTP. F1TDC projects will take some time, but will be finished soon.
→CTP kick off meeting is 2-Oct-2012 with the Zentech folks.
→BOM will be discussed and parts need to be ordered now so any long lead items are available by the time the boards are fabricated.
→Production acceptance test code is at 65%.
→Work by Scott was shown regarding effort at pin swapping to improve routing.

GTP and Global Crate Developments

26-Oct-2012
→Global crate testing s continues. I believe we have all the necessary hardware and stable firmware and library drivers are ready for the production TI-TD. Firmware revisions and drivers for the TS are virtually complete?
→Goal is to completely verify functional operation and performance of the front end crate (CTP), Global crate (SSP→GTP) and the trigger distribution (TS→TD). There are a number of critical and essential timing requirements with full latency of the trigger signal one of the key parameters to measure.

12-Oct-2012
→ECO list prepared for GTP final version
→Work continues with the Global crate test setup.
→2nd GTP prototype has been assembled and tested.

28-Sept-2012
Notes on Global setup and Root development.
Ethernet stack code from Hai appears to work fine and compiles with Altera device.

***ACTION ITEMS*: Next meeting - Friday 2 November @10AM in F226**