12GeV Trigger meeting notes:

13-September-2013: C. Cuevas, A. Somov, N. Nganga, W. Gu, B. Raydo, E. Jastrzembski, B. Moffit

6-September-2013: C. Cuevas, A. Somov, N. Nganga, H. Dong, W. Gu, J. Wilson, B. Raydo

16 August 2013: C. Cuevas, A. Somov, N. Nganga, H. Dong, W. Gu, B. Moffit

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1. Trigger/Clock/Sync – TI/TD

13-Sept-2013

-->Discussion on firmware updates started and William has maintained the updates to the TI, TD and TS. There have been ongoing tests in the Hall D CH area that offer a chance to add features as required for DAQ.

→Good progress on latest features for TS.

→Good discussion on board user manuals, and we should have the DAq group area hold the latest versions. This way we do not have six different sites with six different versions.

6-Sept-2013

→Firmware revisions continue with latest feature of presetting the number of readout 'blocks' that will automatically stop a run.

→We still have plans to setup the final TS and Global crates in the Hall D CH. All the required boards will be configured and tested in the CH before moving them to the hall. There are effectively two TS/Global crate test setups now with one in F117 and the EEL109 lab. I imagine the Trigger test stand will be located in the CH once operations begin.

16-August-2013

→TS boards received, tested and delivered to the hall groups.

→One of the production TS boards is in the Hall D CH and this trigger crate can be populated with SD and TD as needed. We will keep the two trigger crates in EEL109 for a while longer to continue with GTP → TS testing.

-->TIM boards have been assembled and tested. These units are delivered to the Hall groups.

1. *SUB-SYSTEM PROCESSOR (SSP)*

13-Sept-2013

-->Documentation and firmware is complete for the Hall D firmware revision.

6-Sept-2013

→No questions from the uMegas group regarding the SSP.

→The Hall B RICH detector proposal relies on several SSP to readout and controls the front end readout chips for each MAPMT. The review went well and Ben had provided significant information for the previous internal review on the DAQ system.

→Documentation for the SSP continues and the additional trigger processing modes have been finished also.

→The MicroMegas group has received the SSP and other hardware needed to continue their R&D with the GEM detector readout.

16-August-2013 (Ben's update below)

→Hall D Firmware is complete:

1) Trigger processing modes:
   a) summing fiber 0-7 (any combination) and reports to GTP
   b) pass-through fiber x to GTP (for single crates used on SSP that pass directly to GTP)
2) VME firmware update (5.5MByte image):

80 seconds to program time, 15 seconds to verify
3) Monitoring functions
a) scalers on I/O
b) Hall D specific pulse integral histograms
c) serdes bit error monitoring, raw data/waveform capture, data crc

Driver:
I've got a Linux/VxWorks driver that configures the SSP that will be a helpful place for the Bryan to work with so it shouldn't take him long to get it up to par to work with along with CODA.
Documentation:
I'm working on this today and should be completed by end of day...
→SSP firmware (registers) are complete and will need to be given to Bryan for development of the CODA library.

2. CUSTOMERS

6-Sept-2013
→Mode 6 TDC for the PCAL is being used. There are a few issues with the data quality that have come into question by Sergey and other Users. Apparently there are issues with the TDC function and improper timing data is recorded when initially running Mode 6 with the PCAL cosmic setup. Sergey B. has discussed the issues with Ed and Hai. Hai suggests to run Mode 7 to analyze the raw data along with the TDC information.

16-August-2013
→Hall B PCAL group will begin detector tests with the new Mode 6 firmware. After that the FTOF group will use the boards.
→Activity to repair the broken FADC250 production boards has started.
→SBC has been approved to send to CEA Saclay!!

3. "B" Switch - Signal Distribution Module (SD)

13-Sept-2013
→Jobs never done till the paperwork is complete.
Only a few items need to be updated. The 31.25MHz clock will be used for the F1TDC boards and there is a minor issue with the setup of the SD PLL.

6-September-2013
→Nick confirmed that the phase clock difference on start up for different crates is the same. The number of times for turning on the crates is low, but the Silicon Lab PLL operation states that the clocks will be in phase. Additional statistics are not needed and these tests are enough to verify that the PLL turn on state agrees with the datasheet specification.

16-August-2013
→Nick has a brief presentation on PLL testing. Results and test setup were presented and the difference in jitter was understandable. Further discussion let to another test plan to measure phase difference on start up for the front end crates. Use 31.25MHz as the test case because this phase difference may be important for the F1TDC crates.

4. System Diagrams/Fiber Optics

6-Sept-2013
→Elliott would like to combine the Ethernet fiber with the Trigger fiber order for installation in the hall by October. There are many cable trays that still need to be installed before final cable length measurements can be given to the selected vendor.

5. Global Trigger & Trigger Distribution Testing

6-Sept-2013

→Ben is using the production GTP to develop firmware for the CLAS12 tracking trigger. This development will establish experience with the GTP project left over from Scott.
→Low level firmware code has been evaluated/changed by Ben and will continue. Higher level framework from Ben can now be used for the GTP developments.
→Project outline has been drafted by Ben to recruit Chris Hewitt (HPC group) to port an embedded processor on the GTP using Nios. More details will follow, and this could be used for other projects.

16-August-2013

No report.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

6-Sept-2013

-->26 of 33 have been delivered with 8 of the 26 not passing Hai's acceptance test. We will have a phone conference with MTEQ to find out when the last 7 boards will be delivered, and to discuss assembly issues with the boards that did not pass testing.
→Only the 1st article CTPV2 board has passed the FCAT test. Bryan is very busy and the 18 boards that have passed should be run through the FCAT asap.
→There is a long range plan to setup and run the FCAT in EEL109.
→The front panels will be delivered soon.

16-August-2013

→We have a total of 6 production boards with one issue so far on one of the boards. (Clock to U1)
→4 boards can be tested with FCAT and the 1st article production board has already passed the FCAT test.
→Expect delivery of production boards every week until all 32 boards have been received. Vacation plans will stop acceptance testing. Acceptance testing is highest priority.

***ACTION ITEMS*: Next meeting - Friday 20 September 2013 @10:30AM in TBA**