Hall A Moller Polarimeter DAQ Upgrade

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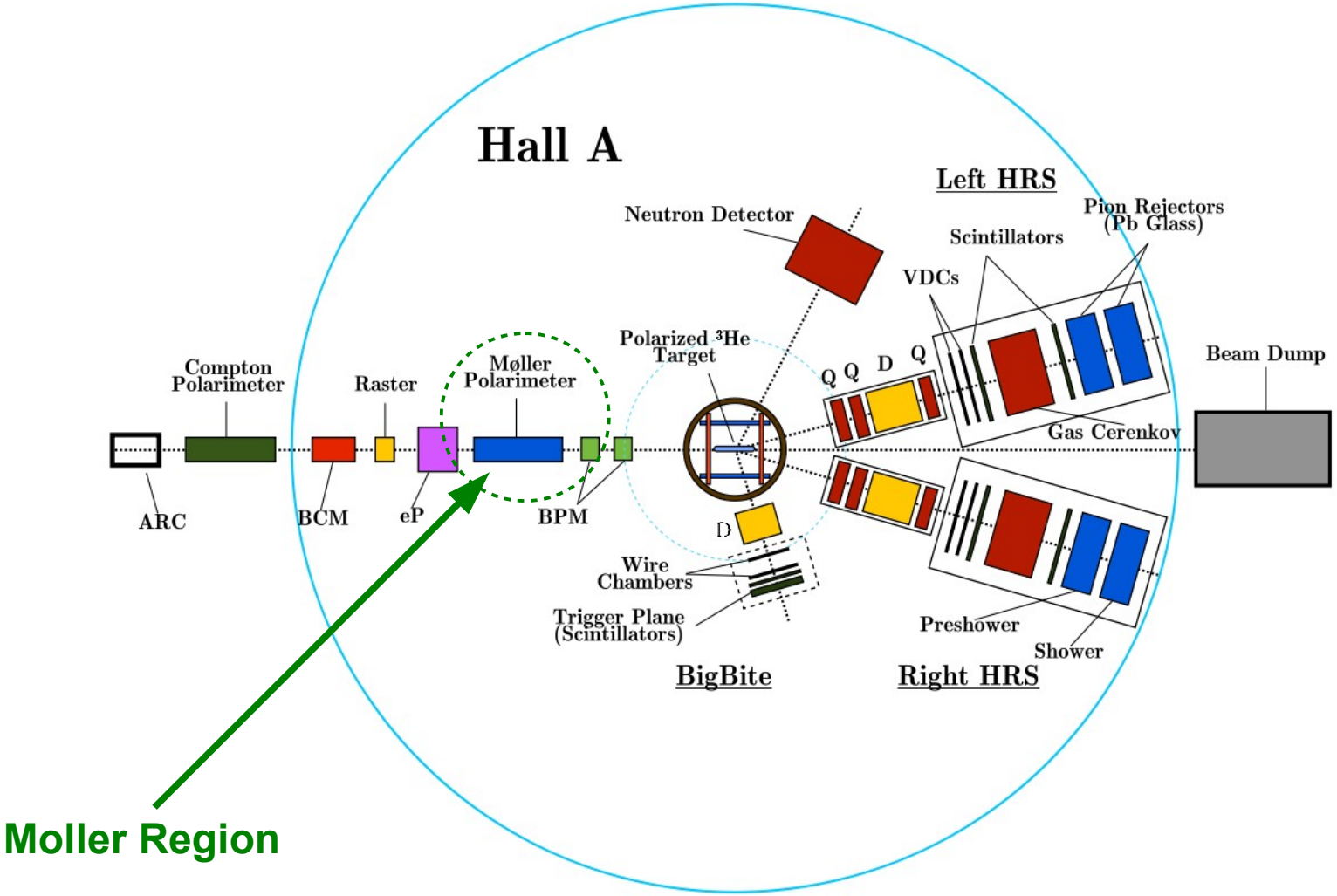
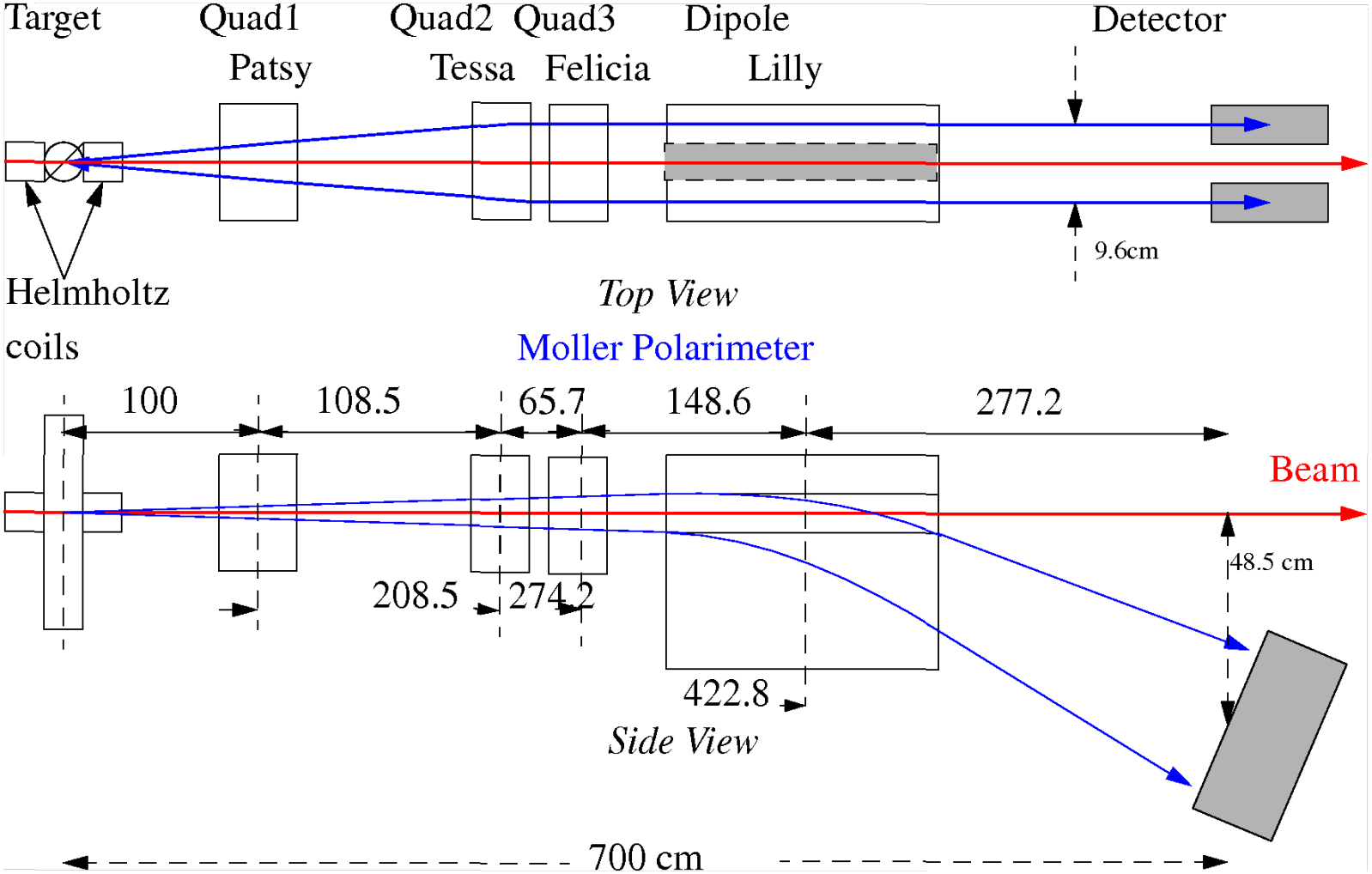
Overview

- Brief description of the Hall A Moller
- What do we gain from the DAQ upgrade?
- What does the DAQ upgrade involve?
  - Hardware description
  - Capabilities
  - Trigger definitions
- Some results
  - Online histograms, rate comparisons, etc.
- Miscellaneous comments

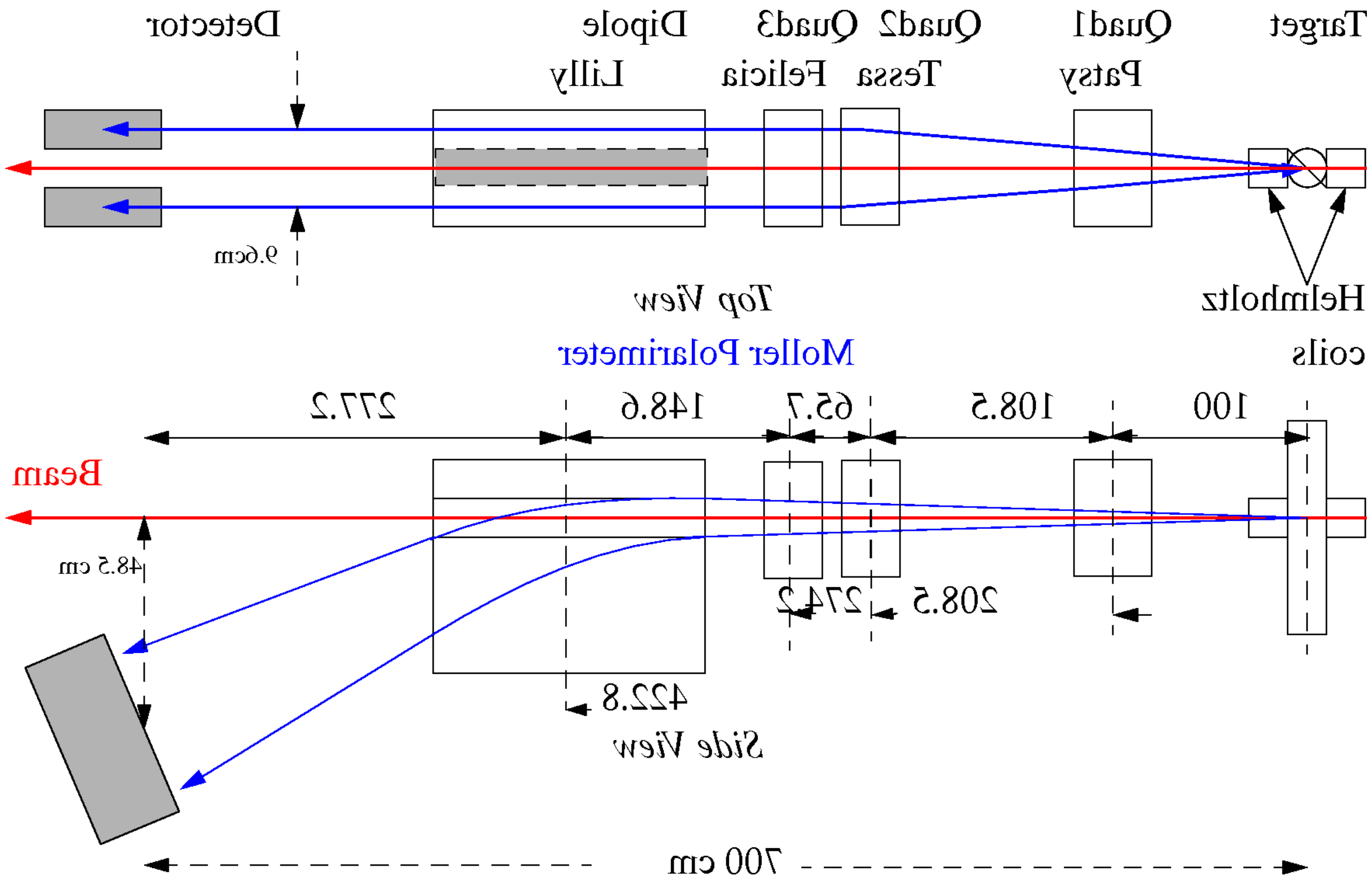
Hall A Overview



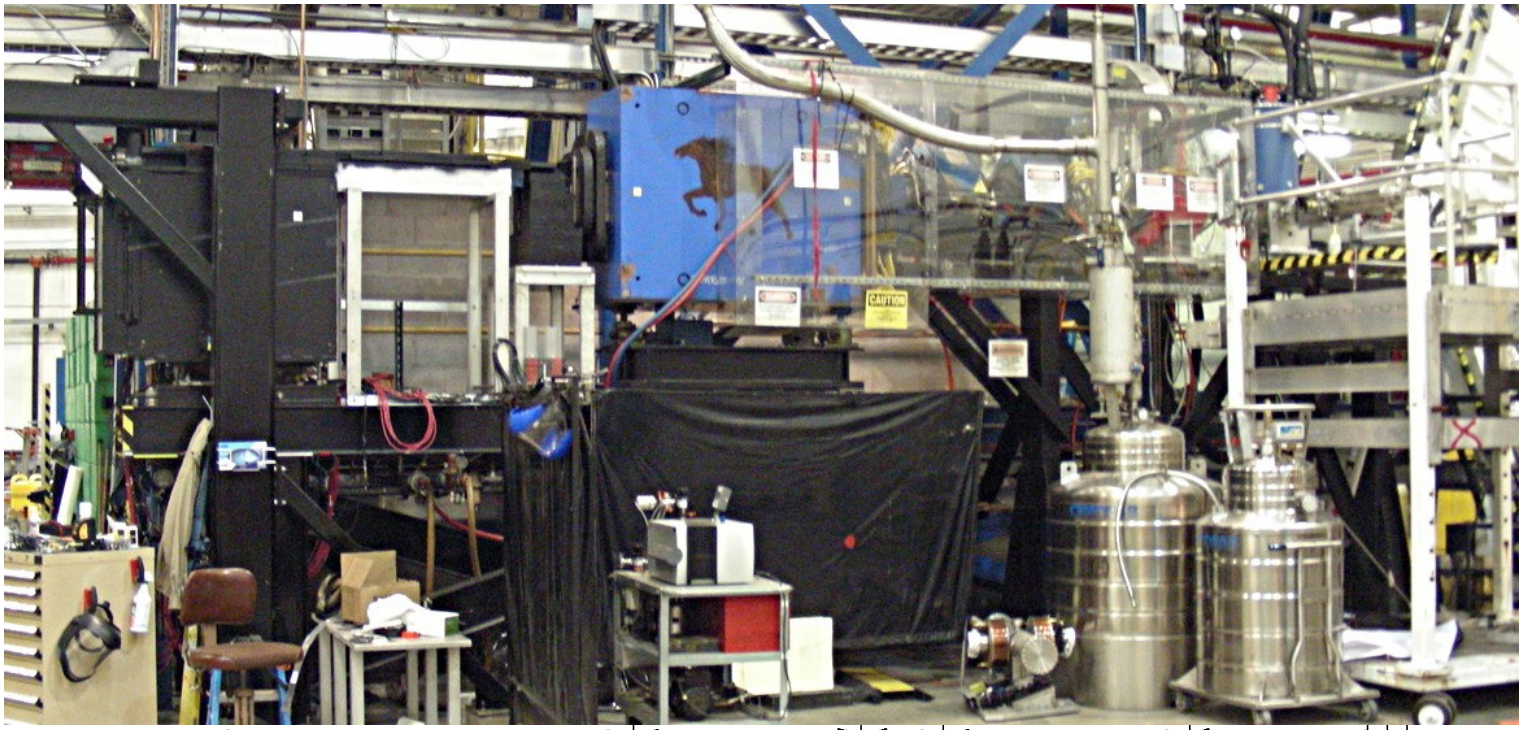
Moller Hardware



Moller Hardware



Moller Hardware



Why do we want the DAQ upgrade?

- Help improve the systematic error from 2% → 1%
  - FADC data grants full information about detector systematics/performance
  - Negligible DAQ deadtime (pipelined design)
  - Intrinsic HW deadtime (ie. pile-up) can be trivially identified/measured using sample data
- Replace old/obsolete DAQ hardware
  - existing DAQ is 12 years old, no spares, rate limited
  - FADC design is fast & flexible
- Accommodate the new segmented aperture detector
  - 8 paddles (4 per arm) instead of 2
  - present aperture paddles overload at > 1uA

What is involved in the DAQ Upgrade?

- System built around a JLab F250 Flash ADC
  - 16 analog inputs (8 calo. blocks, 8 scint. paddles)
  - 4 ns sample time, 12 bits/sample resolution
  - FPGA device → flexibility of software with the speed and response time of hardware
- Custom FADC firmware
  - FADC generates our triggers, no signal splitters, discriminators, or summing modules needed
  - Thresholds, sample windows, trigger prescales all software controlled
  - Fairly straight forward to add new features to the firmware (turn around on the order of a week)

What is involved in the DAQ Upgrade?

- Also some auxiliary support modules (read out during every MPS interval)
  - CAEN v560 scaler (16 channels)
    - BCM, Moller target position, 100 kHz clock
    - (plus redundant counters for cross checks)
  - CAEN v792 QDC (16 channels)
    - MPS, QRT, HEL flags
    - (plus redundant data for cross checks)
  - Easy to add/read other modules if needed

What is involved in the DAQ Upgrade?

- New dedicated DAQ computer: *hamoller.jlab.org*
  - fast, modern machine: 4 CPU cores, 2TB of RAID10 storage for local data and scratch
  - shares adaqfs file system, usual accounts
  - goal is to support zero-deadtime streaming data from DAQ at full 160kHz coincidence rate (no prescaling) → sustained ~50 MB/sec
- ROOT-based analyzer using PODD (Hall A analyzer framework)
  - new decoding routines added to handle FADC
  - still a work in progress, but quite functional

Photo of old DAQ electronics

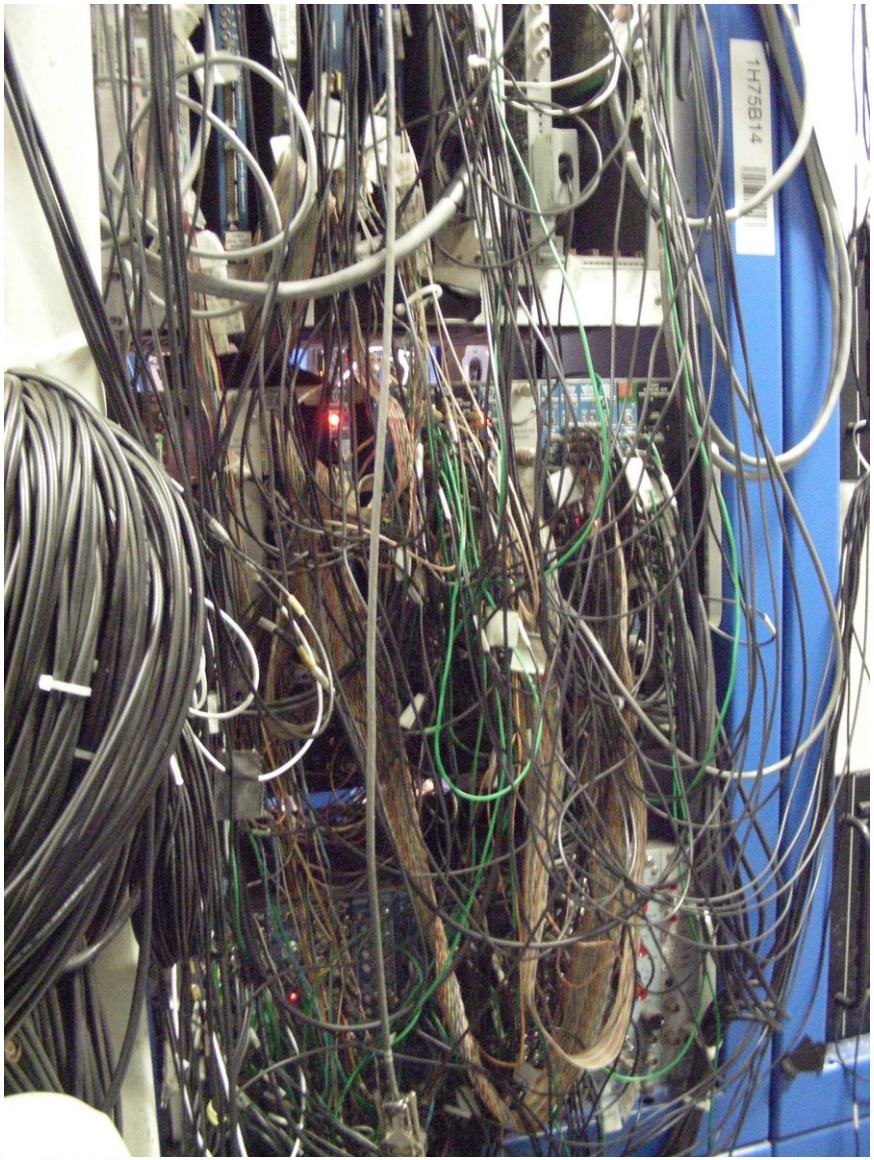
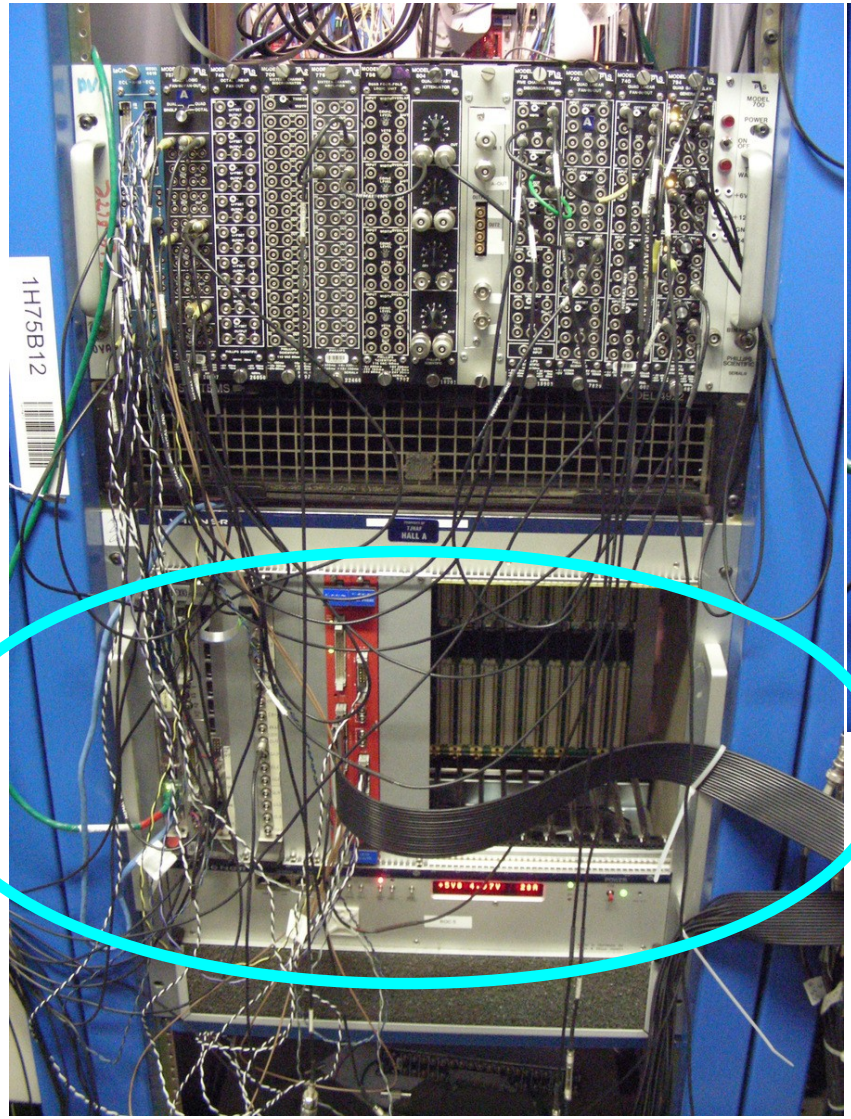
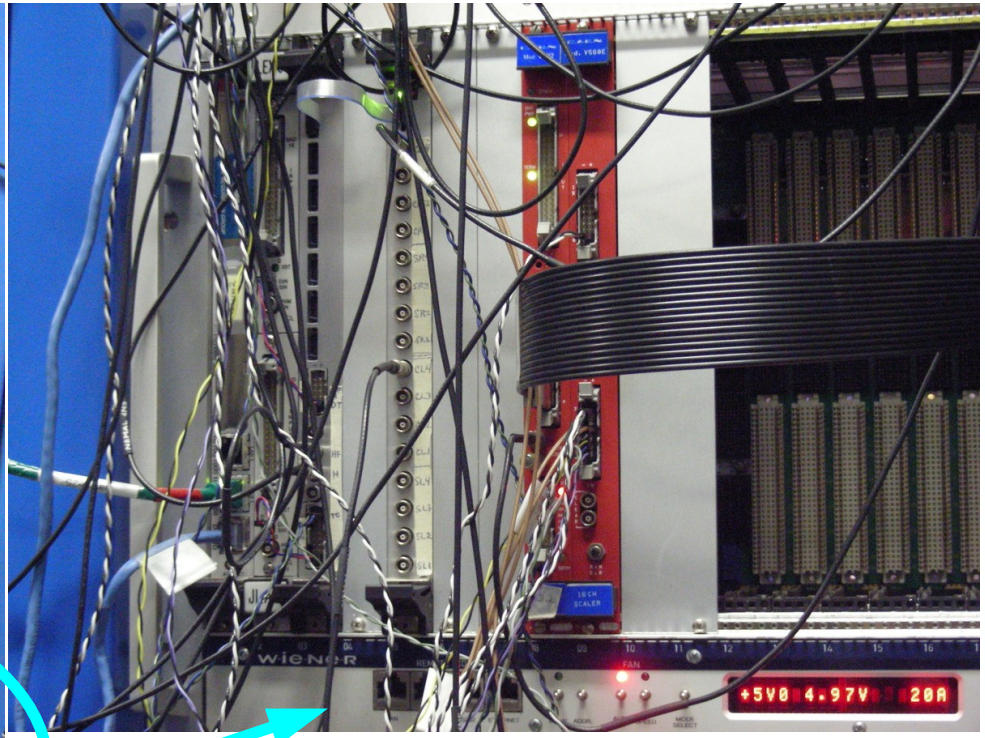


Photo of new DAQ rack





FADC Moller DAQ Trigger Types

FADC internal trigger criteria:

$CR = \Sigma_{I=1,4}\Sigma_{j=1,2} P^J_I > \text{threshold}$

$CL = \Sigma_{I=1,4}\Sigma_{j=1,2} P^J_I > \text{threshold}$

$SL = (\Sigma_{J=1,2} S1^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S2^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S3^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S4^J > \text{thr})$

$SR = (\Sigma_{J=1,2} S5^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S6^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S7^J > \text{thr}) \text{ or } (\Sigma J=1,2\ S8^J > \text{thr})$

'DATA' Trigger (OR of 'internal' trigger cond:):

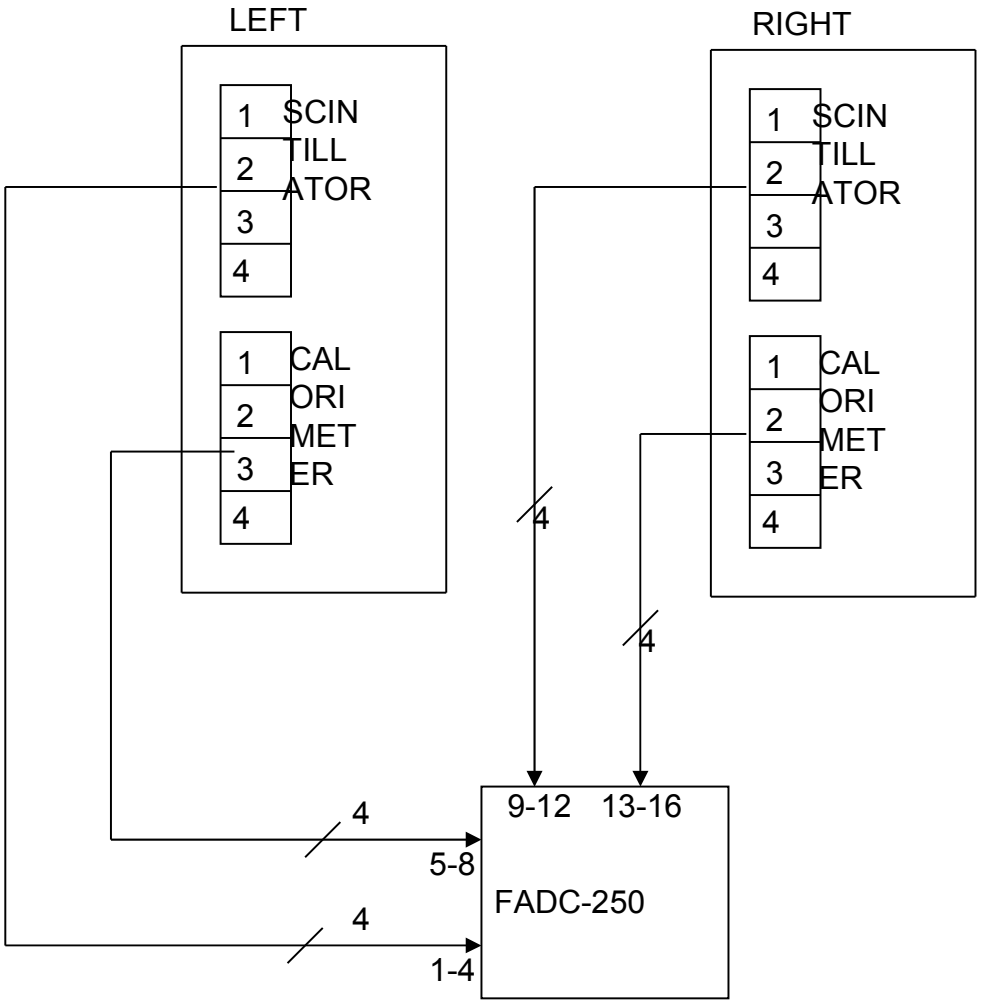
CL.AND.CR prescaled from 1 to 2000
CL prescaled from 1 to 2000
CR prescaled from 1 to 2000

Information recorded:
- digitized waveforms
- helicity state
- status counters, etc.

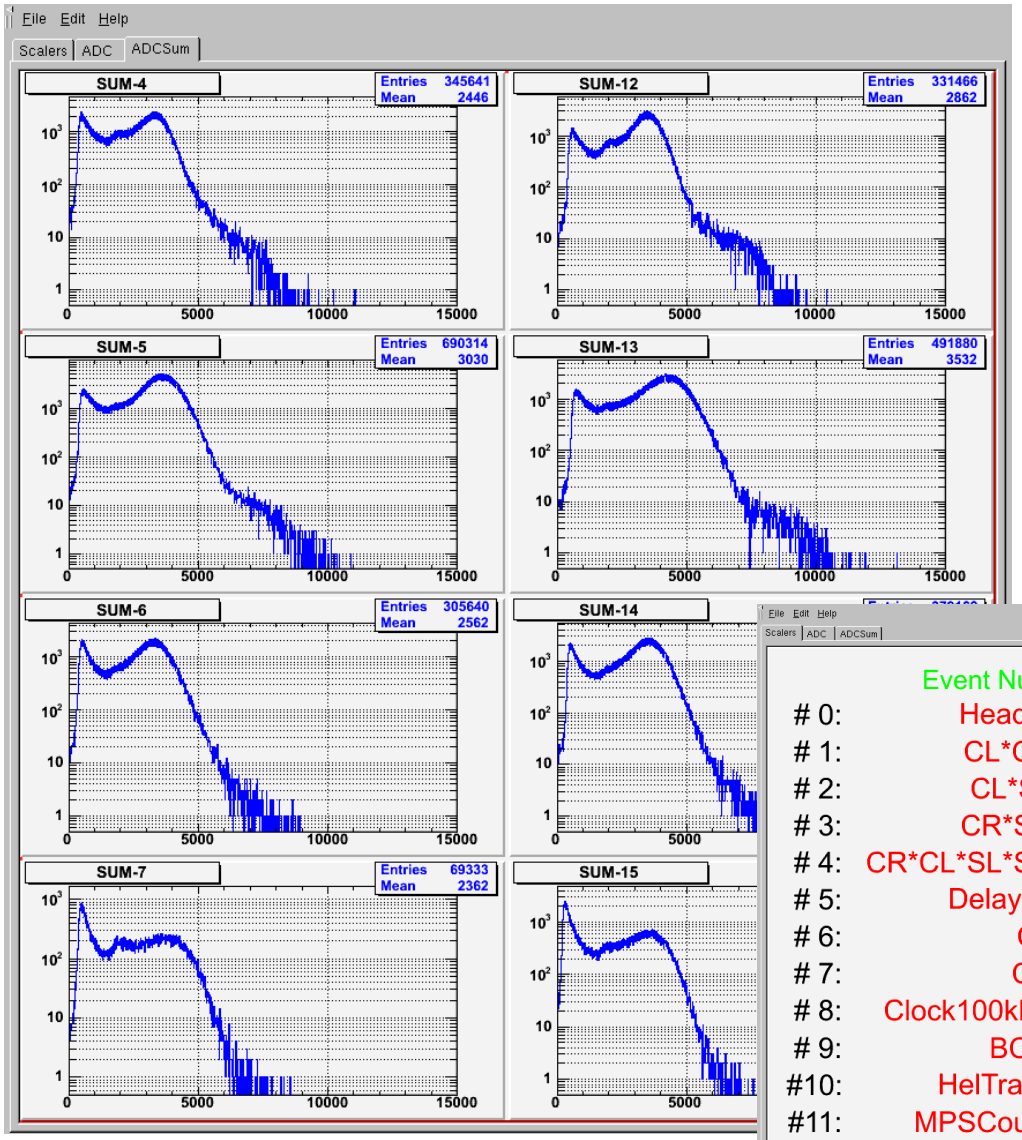
'HELICITY' Trigger (external trigger):

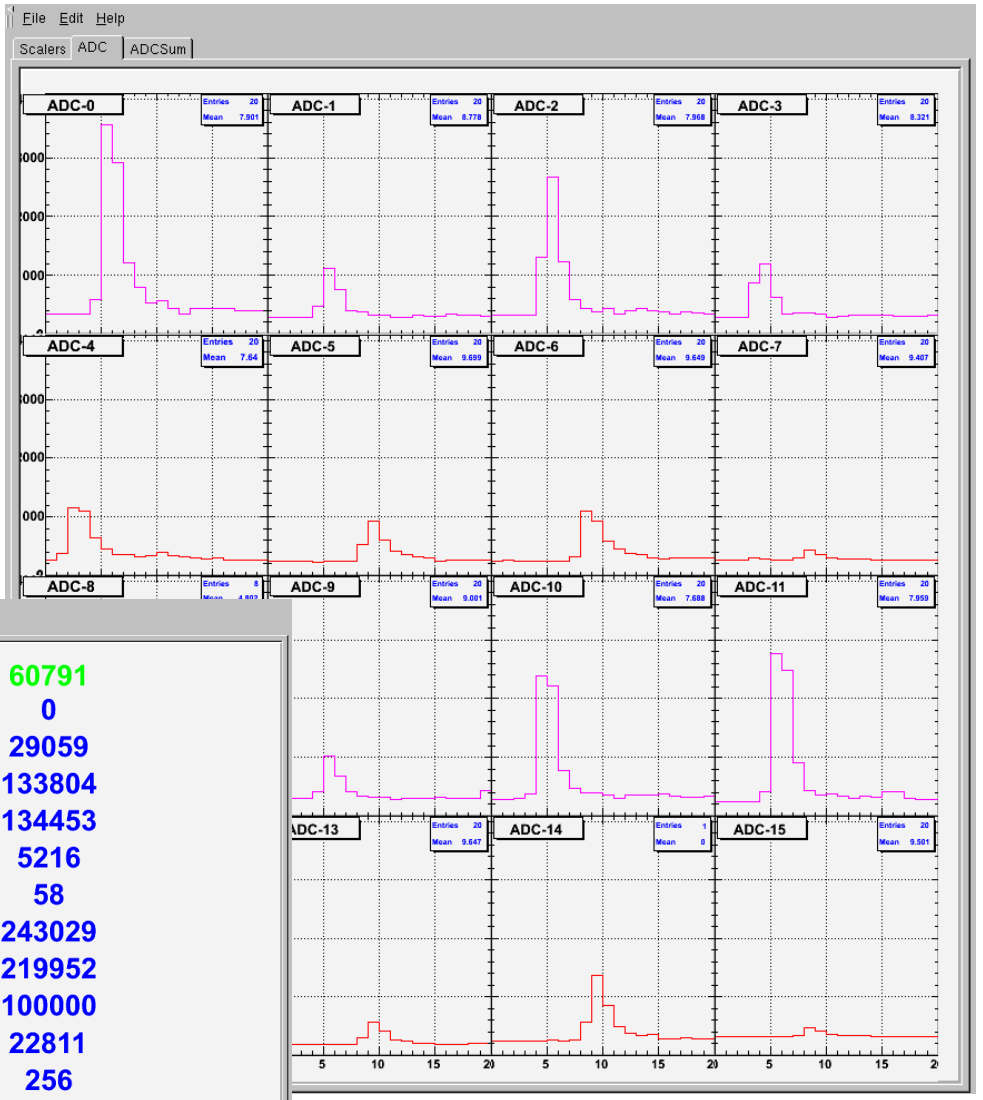
MPS leading edge (30 – 2000 Hz)

Information recorded:
- Helicity, MPS, QRT states, BCM,
- Moller Target ladder position information,
- 100 kHz clock,
- status counters, etc.
- FADC 'Software' scaler data:
  - CL singles, CR singles
  - CL and CR
  - CL and SL
  - CR and SR
  - CL and CR and SL and SR
  - CL and CR and (SL and SR delayed > 100 ns)



On-line FADC monitor

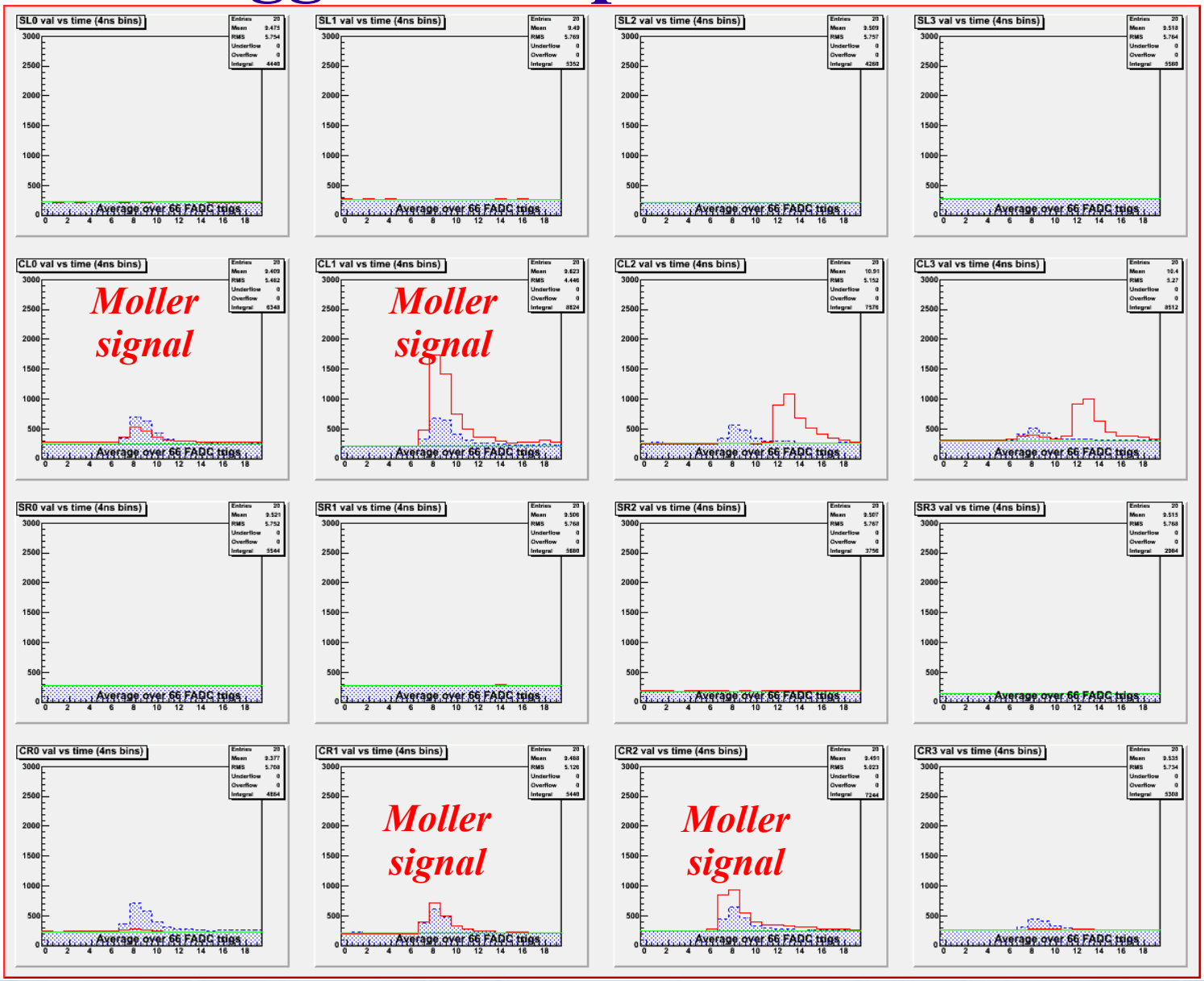




'Data' Trigger example: *Moller + ?*

Cal. 'Left'

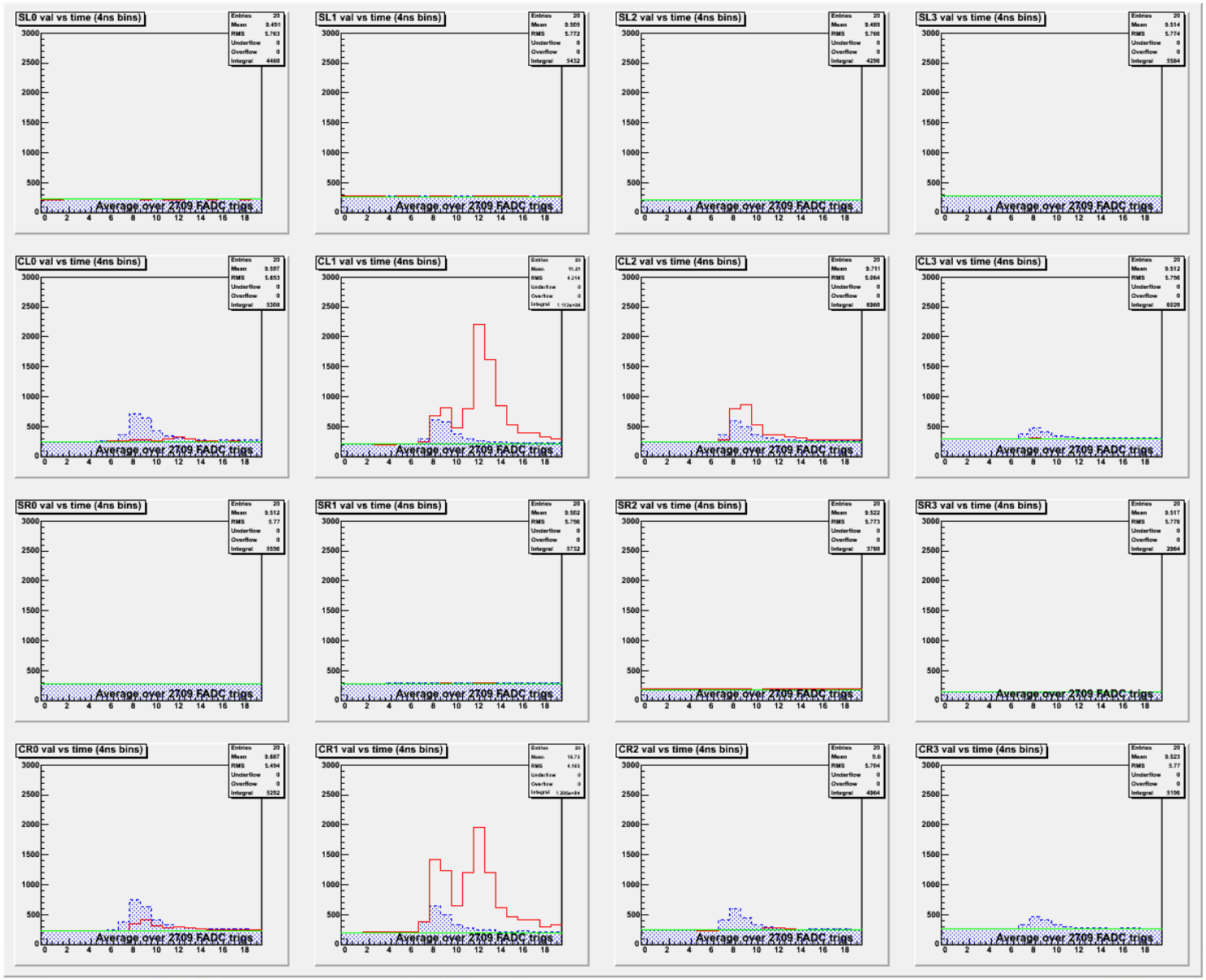
Cal. 'Right'



'Data' Trigger example: *Pile-up Exhibit A*

Cal. 'Left'

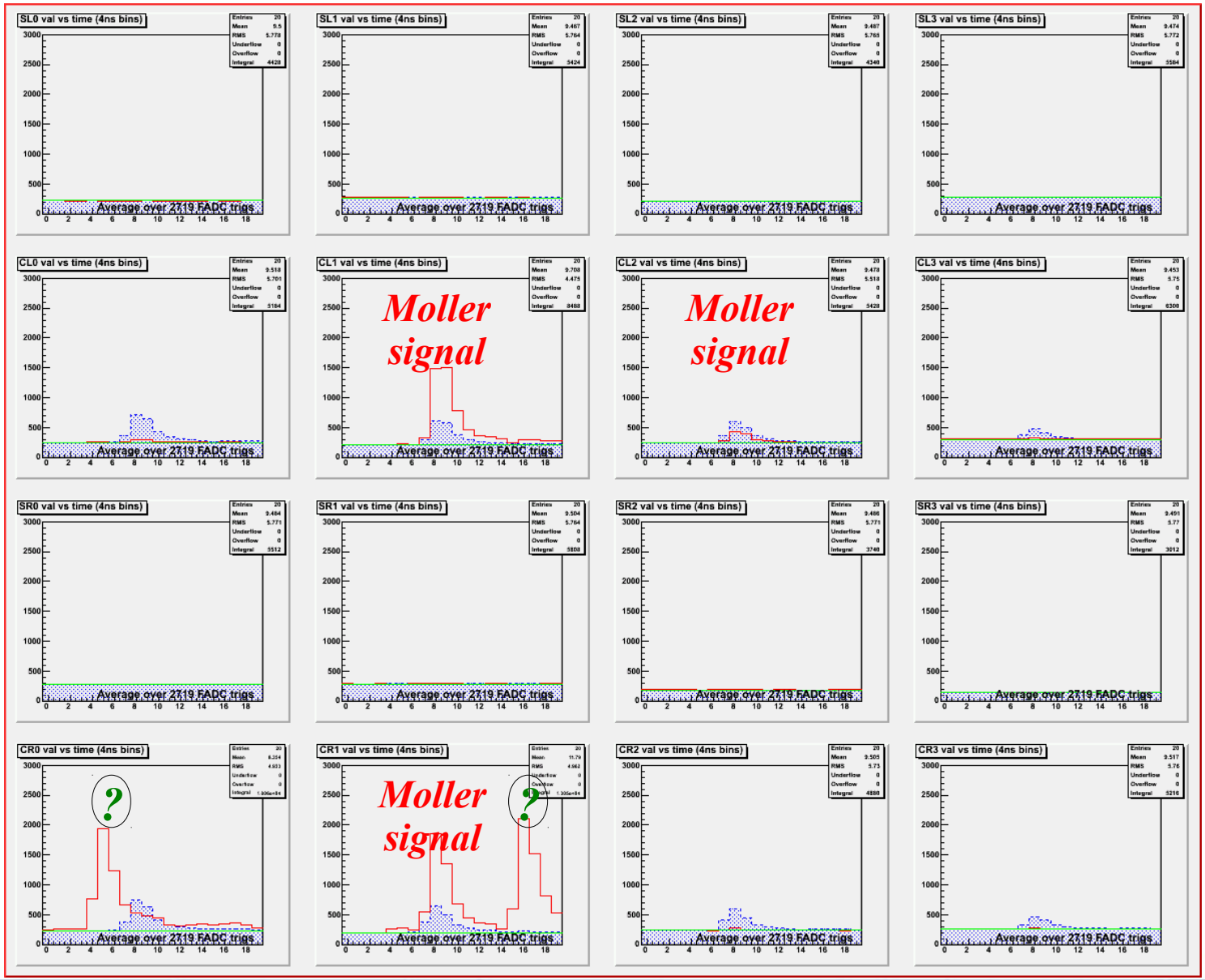
Cal. 'Right'



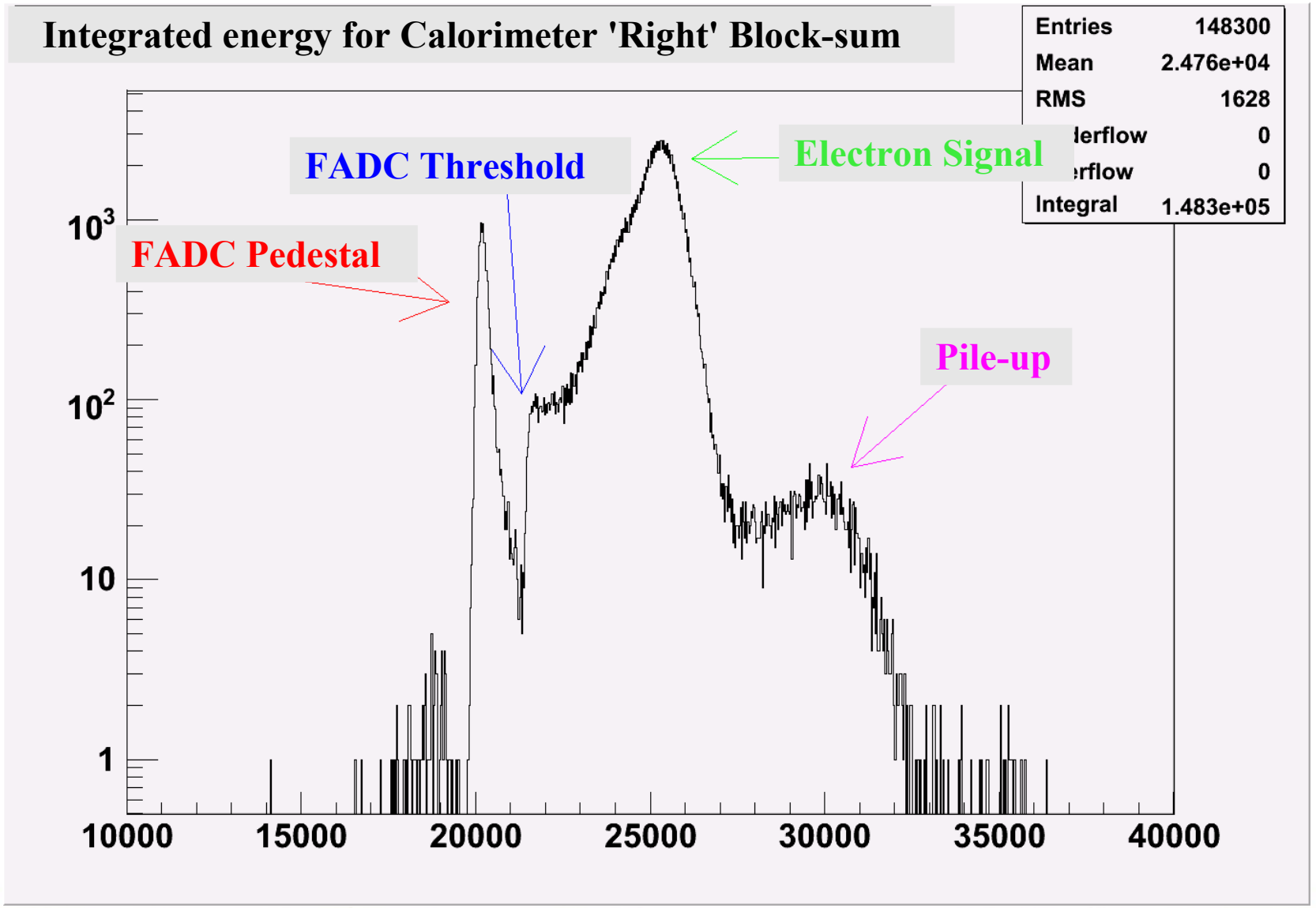
'Data' Trigger example: *Pile-up Exhibit B*

Cal. 'Left'

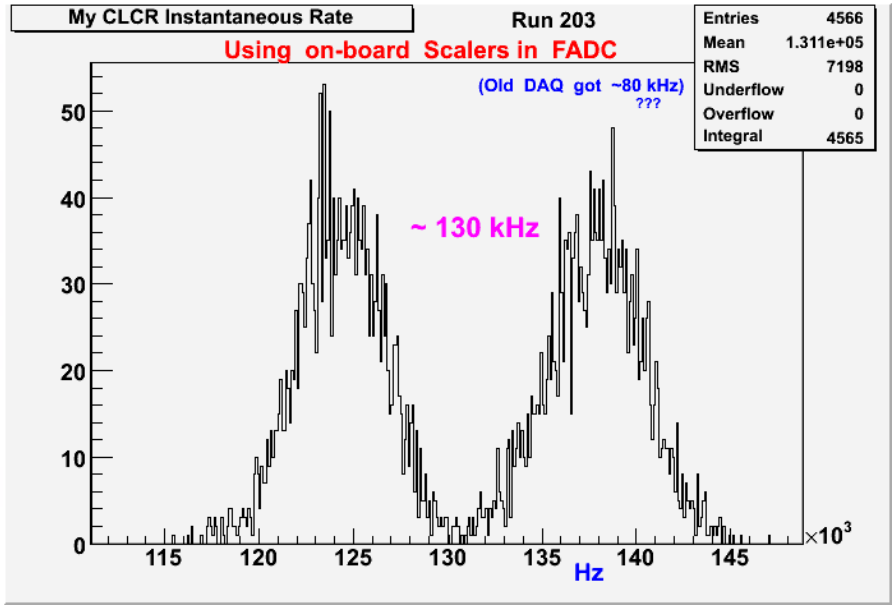
Cal. 'Right'

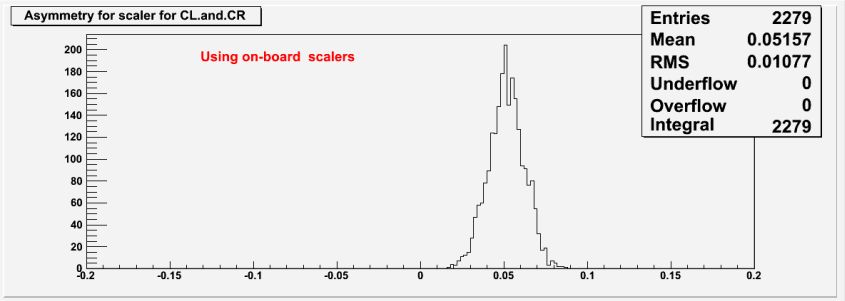


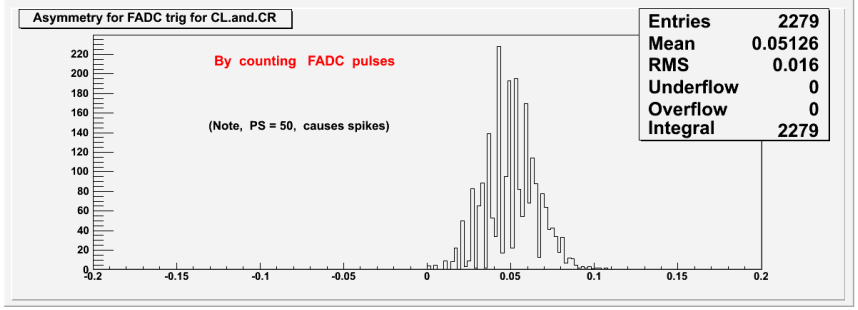
Total Energy Histogram

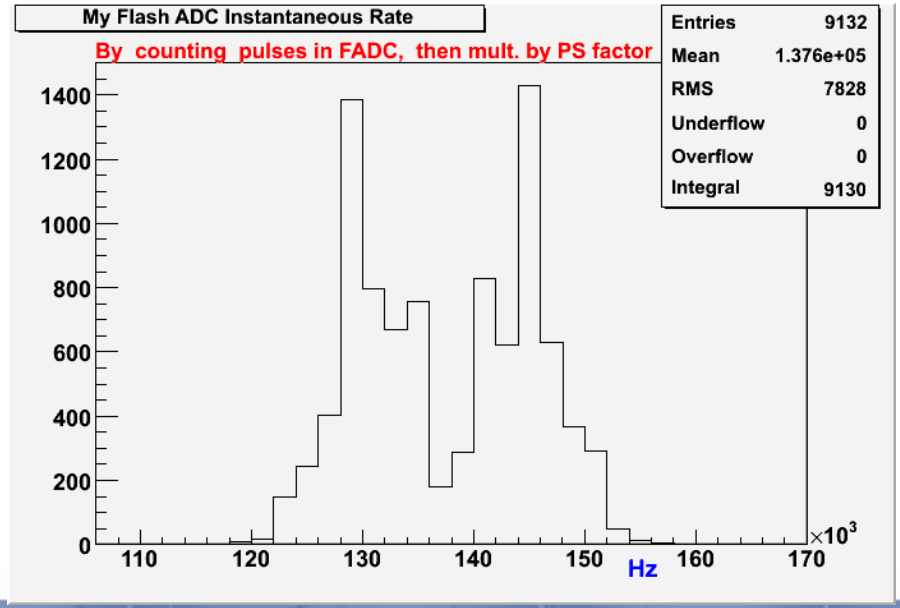


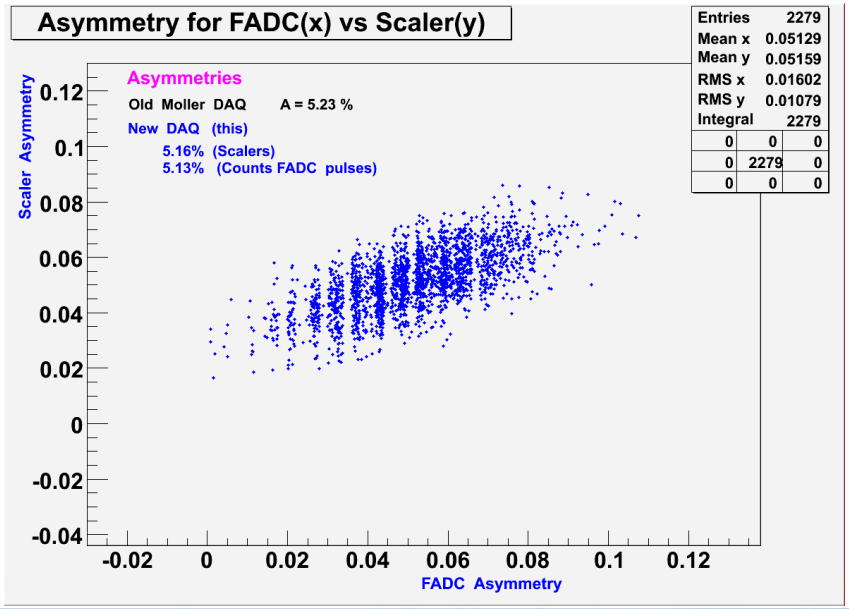
Rates and Extracted Asymmetries





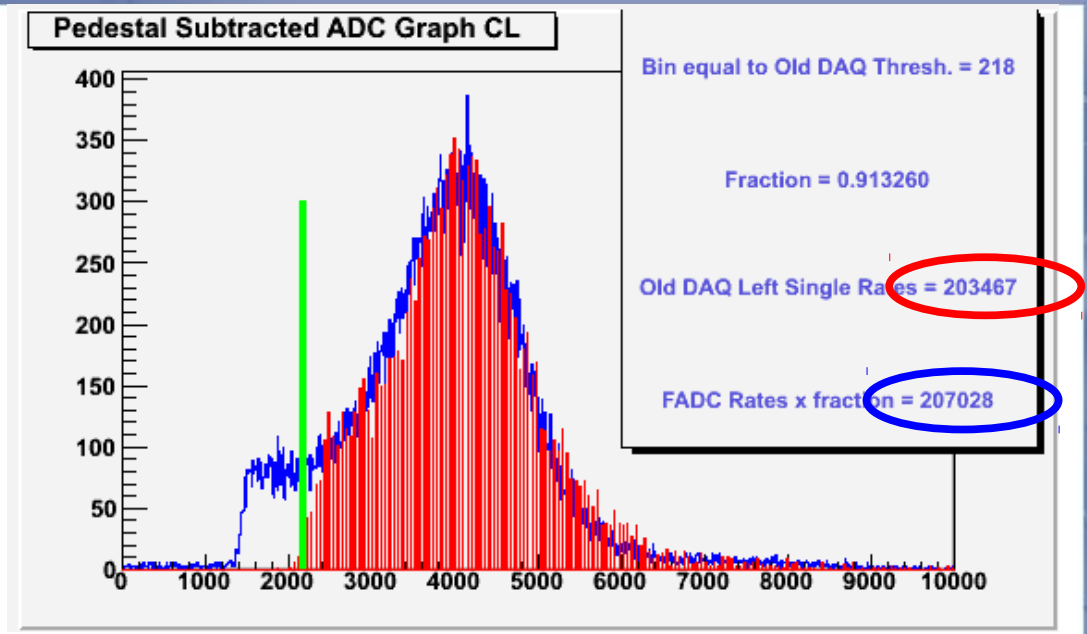




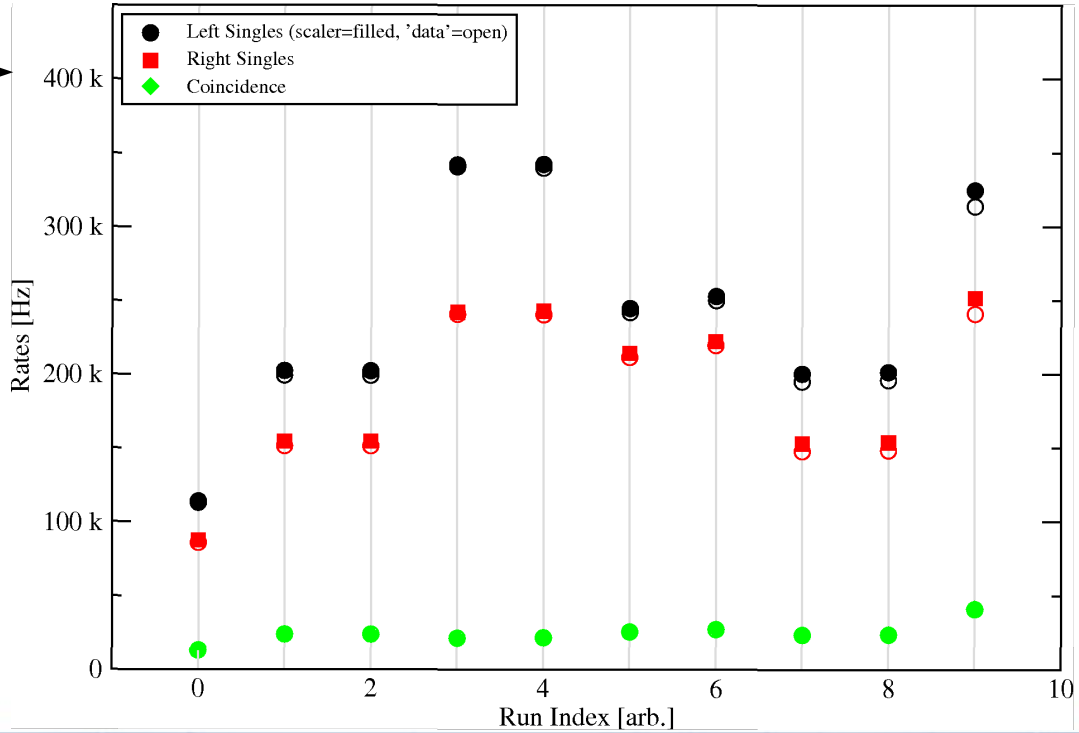


(Recent) Rate Comparisons

FADC
vs.
Conventional DAQ

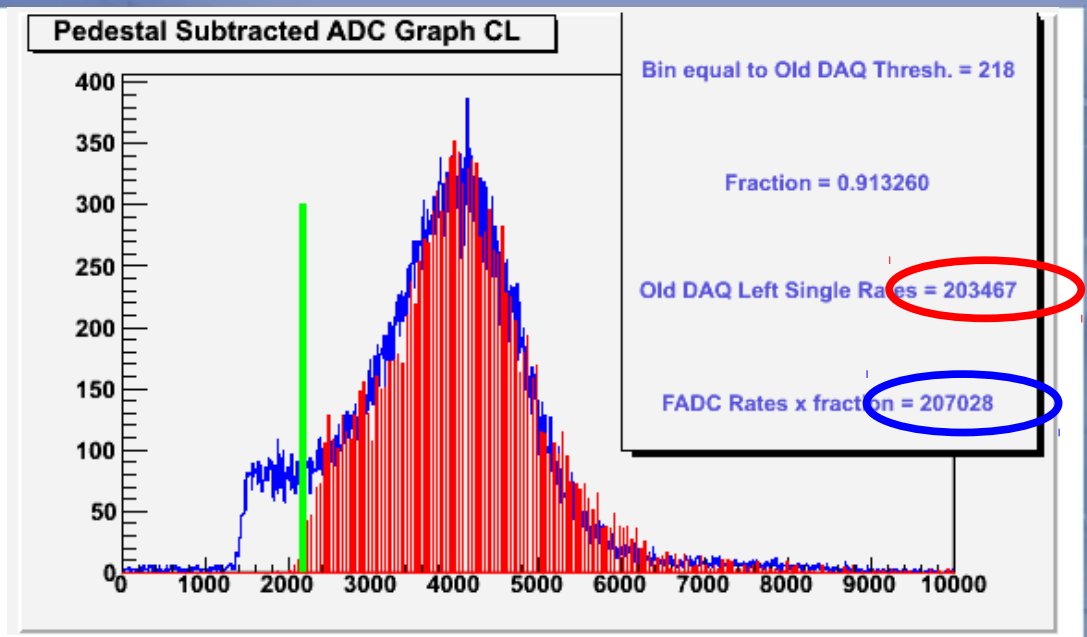


FADC Scaler Rates
vs.
FADC Data Trigger Rates

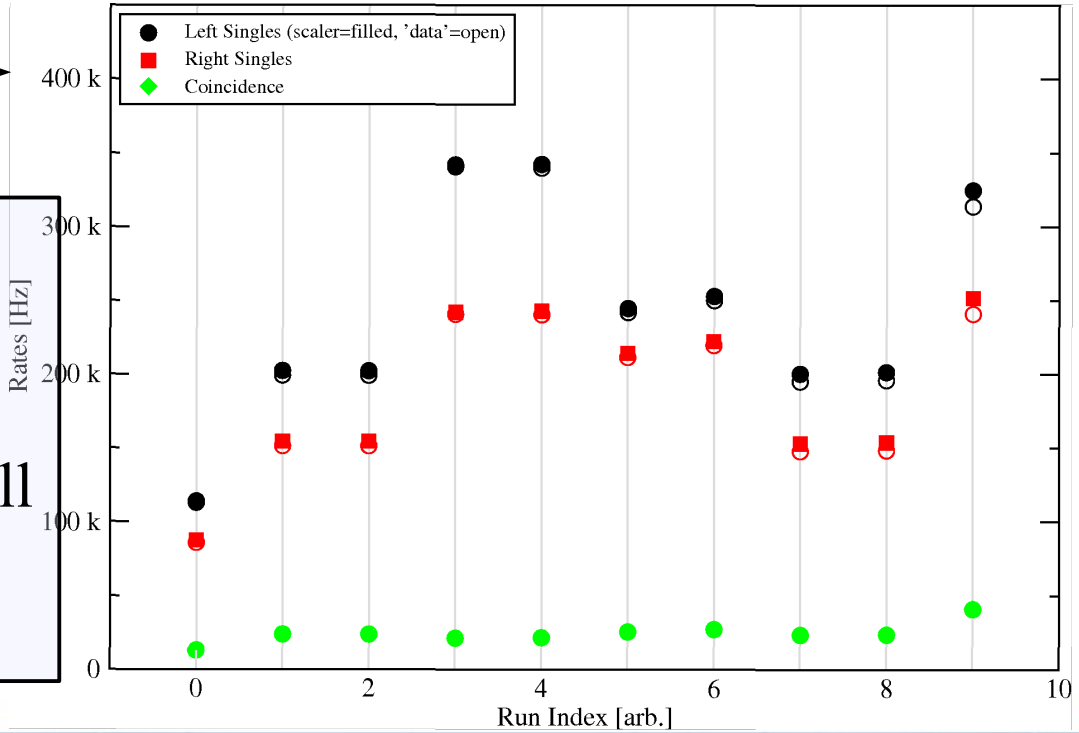


(Recent) Rate Comparisons

FADC vs. Conventional DAQ



FADC Scaler Rates vs. FADC Data Trigger Rates



- Showed deadtime-less operation at >40kHz trig. rate (after prescale)
- Lots of headroom left, will commission those tweaks this summer.

Miscellaneous Comments

- Ran across several interesting features in the FADC that ultimately required firmware updates
  - not unexpected; support from DAQ and Fast Electronics group was great!
  - need to factor in this debug time and additional load on the experts during 12 GeV commissioning
- Radiation Hardness during *PREx* (probably worst-case scenario)
  - FADC250 seemed to survive OK, *but*
  - MVME v6100 CPUs didn't fair very well
    - needed fairly frequent reboots
    - lost 2 of them in two weeks of high-luminosity running (they were upstream, and well shielded too, at least by historical standards)
- Wishlist item:
  - Generic library to decode blocked FADC data → serialized CODA (evio) event stream
  - (perhaps impossible to provide general solution...)