# ***12GeV Trigger meeting notes:***

30-Nov-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga

23-Nov-2012: No meeting—Thanksgiving holiday

16-Nov-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga, B. Moffit, E. Jastrzembski

9-Nov-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga, B. Moffit

---

## 1. *Trigger/Clock/Sync – TI/TD*

**30-Nov-2012**

-->All production boards have been delivered!
→Minor assembly work is being completed here, and each board will need to pass the acceptance test.
→Acceptance testing has started.
→TS CODA library is under development by Bryan.

**16-Nov-2012**

-->20 TD boards have arrived, and 5 have been tested.
→20 TI boards arrived with 2 boards fully tested.
→The P0 connectors should be installed and only a few will have the P0 omitted. Check the SFI to be sure that there is full clearance for the TI with P0.
→Bryan has the updated CODA driver library for the production TI boards and removed the old driver from the site directory.
→TS testing is progressing, and there seems to be an issue with the VXS crate that has the Elma 20 slot backplane. Production boards should be ready to order by March-2013.

**9-Nov-2012**

→1st article boards will be delivered to customers next week. (Hall B)
→Production deliveries "should" begin next week also. Not clear how many are in a 'lot'.
→Rate register implementation would be nice and useful, but presently the rate is calculated from reading registers at a fixed interval. Counters could be implemented on board to produce a "Rate" that merely has to be read from a register.

**2-Nov-2012**

→Acceptance test procedure code is proceeding well.
→No news is good news and no update from CEM regarding the production board delivery schedule
→Rate measurement registers? Check to see if this is already included on the trigger boards. TS board will have this feature, and it could be added (if not already there) on the other boards.
→Sounds like requirements to me,,,,, TS 'shall' include deadtime measurement. Does this exist on the TI? Firmware exists for SSP and may be re-usable for other boards.

## 1. *SUB-SYSTEM PROCESSOR (SSP)*

**30-Nov-2012**

→Fabrication data was delivered to Zentech last week and the bare boards will be ready soon. Schedule for the 1st article should remain on track.
→Front panel design files and firmware activities are progressing.

**16-Nov-2012**

→2 week turn for bare board, then about 1 week for assembly. 1st article production SSP will be delivered soon after the assembly is complete.

→uMegas (Saclay) folks have requested a SSP board and several other trigger board hardware for their test setup in France.
→Firmware modifications for the production boards are progressing and will be ready for the 1st article testing.

**9-Nov-2012**
→SSP production files have been shipped!! Several people reviewed the files and no show stoppers.
→All components have been ordered by Zentech, and an update for assembly will be delivered soon. 1st article due and 10 days for testing to approve the remaining units.

## 2. CUSTOMERS

**30-Nov-2012**
→A discussion regarding the existing single board computer order was started, and it the focus was regarding the implementation of the PO connection from CPU vendors that are under consideration.

The PCIe protocol appears to be the method that the Concurrent vendor uses, and the plan is to wire at least one full duplex lane from "PP17" on the CTP board. It is not clear how this PCIe lane will be implemented yet, and there may be limitations on the functions/data transfer that can be supported on the CTP.
→Not certain what the status is regarding the full crate testing that is set up in F112. At the last meeting Bryan had made significant progress, and no show stoppers were mentioned. FADC250 boards should start arriving to JLAB soon.

**16-Nov-2012**
-->1 full duplex lane will be routed from PP17 to the CTP. This is already on the schematic, and Hai has plans to implement the PCIe from the Concurrent CPU.
→More details on the PCIe implementation will be forthcoming.
→5 fully populated crates are in F112 ready for testing. Input range switches need to be verified, including VME address switches.
→Procedure :( Three main sections below)
-"Pedestal" operation. No input cables, and raw data are produced to read back each channel offset and baseline 'noise'.
- All 16 payload boards in the crate, setup with "playback" mode test (all channels), Playback mode (partial occupancy)
- Deterministic alignment test with trigger data passed to the CTP

**9-Nov-2012**
→Executive decision to implement all four lanes from PP17 to CTP! It is copper traces and 16 capacitors. Transceivers "should" be available.
-->Full crate testing will be performed in F112 and Bryan has the software at the 85% level. The FADC250 boards will be arriving from UMass soon, and the full crate testing will take about an hour for each crate.

**2-Nov-2012**
→Intel i7 cores, generation 2 are on order. (16) These will be distributed to the hall groups for detector test setups and evaluation.
→Generation 3 boards will probably be the single board computer (ROC) of choice for the production version.
→PCIexpress is used on these ROCs from Concurrent. VITA 41.3 is supported. These lanes have been considered for the CTP and GTP and the plan is to implement these connections on the boards. Is a PCIexpress IP core needed?

## 3. *"B" Switch - Signal Distribution Module (SD)*

**30-Nov-2012**
-->Firmware for SN storage and readback is a work in progress. Other projects are taking priority. The Trig_Out logic would be a very useful feature to develop, but again, other 'non-trigger' projects will take priority.

**16-Nov-2012**
→3 repaired boards have been delivered and are working! 100% complete!!!
→Firmware for the SN storage and readback is about 90% complete.
→Trig_Out logic firmware is the next project to complete.
→Implementing the SD→TI link will be another firmware project to complete in the near future.

**9-Nov-2012**
→2 repaired boards will be delivered next week. These will need to be tested.
→Firmware will be updated to include the SN of each board.
→SN will be readout from SD through an I^2C register.
→To do: Consider solution for SD→TI link path
FPGA firmware download through I^2C
65K LUT for Trig_Out logic

**2-Nov-2012**
→No update on when the repaired boards will be delivered.
→Hall B SD boards are in the EEL109 locker and at least 4 delivered to the CLAS12 SVT group.

## 4. System Diagrams/Fiber Optics

**30-Nov-2012**
-->Send PR today for approval. This order is for both Halls D and B, and only includes patch cables and patch panel hardware. The trunk line order will be later in the spring when the cable trays are installed.

**16-Nov-2012**
**Get the PR written and submitted! (Panels and patch cables only for Hall B & Hall D)**

## 5. Global Trigger & Trigger Distribution Testing

**30-Nov-2012**
→There are a few minor things to complete to get the three crate global test running. Bryan has been very busy with other projects, but all the hardware is in place.
→Firmware is progressing and a full GTP coda library has not been started.

**9 and 16-Nov-2012**
→Scott has slides
→There are three crates in EEL109 and the Global Crate test is configured. Scott presented his latest measurements and the slides are attached.

**2-Nov-2012**
-->Global crate testing is progressing nicely, and the three crate setup is almost complete. All four GTP (Densishield) output cables will be routed to the TS soon.
→5Gb/s discussion
→Interface work and GUI implementation is still in development and progressing.
→Further discussions on initial global trigger functions and future requirements. Upcoming Lehman review will definitely show that the hardware has plenty of resources to handle the

future requirements. Examples are expanding the simple BCAL from summing only to a cluster finding algorithm.

**20-JAN-2012 (Keep this date to reference full DAq crate procedure)**
**3-June-2011**
***→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***
**16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.**

## 6. Crate Trigger Processor (CTP)

**30-Nov-2012**
→32 CTP have been awarded to MTEQ. BOM should be ready to send next week.
→Circuit board routing is progressing nicely and should be ready for full verification soon. The goal is to send the manufacturing files to MTEQ before the JLAB holiday shutdown begins.
→PP17 is routed on the CTP with one full duplex lane. Need to discuss how this will eventually be implemented, but for now the routing is the main focus.
→Check on the routing status.

**16-Nov-2012**
Bids are due today!
→The latest routing file looks good and there are a few changes to the regulator/power section of the board that remain to be completed.
-->Internal fabrication file 'review' 1st week in December?!

***ACTION ITEMS*: Next meeting - Friday 7 December @10AM in F226**