12GeV Trigger meeting notes:

13-Dec-2013: C. Cuevas, W. Gu, B. Raydo, A. Somov, B. Moffit, E. Jastrzembski, H. Dong

6-Dec-2013: Canceled

29-Nov-2013: Thanksgiving holiday

22-Nov-2013: C. Cuevas, W. Gu, B. Raydo, A. Somov, B. Moffit, E. Jastrzembski, N. Nganga, H. Dong

15-Nov-2013: Canceled

8-Nov-2013: C. Cuevas, E. Jastrzembski, W. Gu, B. Raydo, H. Dong, A. Somov

1-Nov-2013: Canceled

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1. Trigger/Clock/Sync – TI/TD

13-Dec-2013

Discussion on implementing the FCAL cosmic test. The production SSP and CTP should be tested in F117 before moving these boards to the hall.
→TS -→TD crate is ready to move to the hall. Firmware for TD <-> TI ID information is ready. Not implemented in CODA3.

22-Nov-2013

→Initial FCAL DAQ/Trigger configuration will use two TI-Masters and possibly one SSP for these crates.
→FCAL trigger fiber needs to be measured for final length. Will check to see if all cable trays are in place, measure, and then order.
→Discussion continues for the TI-TD link information. Sounds like the details need to be documented. This is not a high priority job, but will be essential by the time the full DAQ system is commissioned.

8-Nov-2013

→New TS firmware is ready for deployment with V9.1 as the latest revision.
→Continued discussion about defining requirements for the crate/port information that will be very useful for the TI->TD links, and hopefully these details are in a document or appended to the TI-D manual.

25-Oct-2013

→Discussion started regarding the fiber port mapping and new requirements for information between CTP->SSP and TI->TD that define the port map and crate ID. This type of information is not presently in the communication link between CTP→SSP nor TI->TD.
→I believe there has been some discussion with Alex regarding the definition of each trigger bit. Some discussion started about asynchronous triggers, but I did not record good enough notes. What input bits will be considered asynchronous? Or will all inputs to the TS be considered asynchronous?
→William has delivered the TD and TS boards to the Hall D group. The TD boards use the geographic pins from ‘64x so there is no need to set addressing switches. The fiber transceiver ports for each TD will be populated, so in principle the TD→TI links can be arranged from left to right, and top to bottom. Detector subsystem front end crates (TI) will be assigned to the TD slot and port number.

1. SUB-SYSTEM PROCESSOR (SSP)

13-Dec-2013

-->Define registers for ID information between CTP → SSP links. Presently this ID info is not implemented. Lower priority, but from my understanding of the discussion this ID info should not be too difficult to define, implement and test.

22-Nov-2013

→The CTPV2 to SSP test needs to be tested, but the firmware and CODA driver is ready. Need to propagate the new firmware to the boards in the hall and other test stations.

8-Nov-2013

→The global crate remains in EEL109 and we are well into November, and this crate appears to be ready for delivery to the hall. Are the CODA libraries completed for the SSP?
→Ben and Alex have defined the (crate) input fiber port mapping for each of the SSP.

2. CUSTOMERS

13-Dec-2013

-->Modifications are still pending for the 'Mode 6', bugs identified and further testing will be required before final version released. Firmware modifications should not require any library(driver) changes.
→I believe the PCAL folks (Hall B) could still be the 1st detector group to use this Mode 6 with a full crate of FADC250.

22-Nov-2013

→Continued work on the Mode 6 modification and testing.

8-Nov-2013

→I believe Ed has produced several playback waveforms that reproduce the errors with the high resolution timing mode. (Mode 6) Hai will need to use the playback data from Ed to verify his Mode 6 firmware changes.
→After Mode 6 firmware verification is complete, the new applications (see notes from 27-Sept) will need to start.

27-Sept-2013

→Priorities:
CTPV2 testing
Mode 6 repair
BCAL cosmics
Tagger Hit bit application
TOF application
Pair Spectrometer
CTPV2->SSP ID

3. "B" Switch - Signal Distribution Module (SD)

13-Dec-2013

→Revision A5?

22-Nov-2013

→(757) Northrup Gruman! We cannot afford Nick's consultant fee. Congratulations Nick!

8-Nov-2013
→Nick modified his firmware to fix a few issues discovered when running FCAT on a crate of F1TDC boards.

4. System Diagrams/Fiber Optics

13-December-2013
-->5 of the 11 fiber trunk lines have been installed. (Thanks Armen!) Will need to test each one when we return from the holiday break.
--> The long fiber lengths from the Trigger rack to the FCAL, and to the Tagger tunnel area have been measured by Tom's group. Will order upon returning from holiday break.

8-Nov-2013
→It has finally happened,,,5 of 11 fiber trunk cables have been ordered!! Will need to coordinate installation with Tom Carstens (Hall D) and will also need to measure lengths for the FCAL and Tagger tunnel areas. Fortunately the cable is a stock item, and it will not take long to install and test the short lengths.

5. Global Trigger & Trigger DistributionTesting

8-Nov-2013
→I do not have notes from the meeting for this section. May be a good idea to invite Chris Hewitt to a meeting for a brief presentation on the embedded Linux project.

25-Oct-2013
→Chris Hewitt can begin work for the embedded Linux on the GTP.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point)See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

13-Dec-2013
-->8 boards delivered to MTEQ on 9-Dec-2013 and we already have a rework plan from them and several of the boards have been sent to a sub-contractor for 3D Xray. We estimated that these boards should be back to JLAB by 17-Jan-2014.

8-Nov-2013
→25 of the 33 production boards have passed acceptance testing and are loaded with the latest firmware. Hai has completed testing of the remote firmware download feature, and the working boards have been delivered to Hall D. (Alex)
→Preparations to send the boards that need rework back to MTEQ are underway and by 9-Dec-2013 we will ship these CTPV2 boards using a new RMA. Round 2!

***ACTION ITEMS*: Next meeting -Friday 20-December 2013@10:30AM in L210A**