### Main characteristics of JLab discriminator

- 16 Channel discriminator each channel is splitted into 2 Independent channels with separate
  - Thresholds (-1023 to 0 mV)
  - Pulse width (4 to 40 ns)
  - Delays ( 0 to 1016 ns with 8ns steps )
- Scalers (125 MHz)
  - Gated (Ext. NIM), Ungated (100% gated)
  - Trigger, TDC (dECL output)

## EPICS driver desired requirements

- Set and monitor at ~2 Hz the
  - Thresholds
  - Pulse widths
  - Delays
- Read scalers at 1 kHz
  - Set scaler configuration parameters like FIFO length, sampling time, etc..

NB: This should be done without interfering DAQ

### Discriminator/Scaler Block Diagram **General Notes:** Common 1) VME Accessible Elements: TRG Thresholds, Pulse Widths, Width Delays, Masks, Scalers, Firmware, Calibration 2) NIM I/O: LEMO coax Dual threshold 3) dECL: 34pin 0.1" dual row header channel TRG Threshold L.E. Disc Pulser Analog 0 to -1023mV 4 to 40ns 16 Input L.E. Disc Pulser 0 to -1023mV 4 to 40ns TDC Threshold x 16 Channels Common TDC Width **FPGA** Scaler Event Builder 64x VME Controller A24/32 - Calibration values BLT32, BLT64, 2eVME, 2eSST Test NIM - Self-calibration logic +5V, +12V, -12V - Firmware management - DAC controller 32 Input OR NIM Maskable OR Delay Scaler Scaler 0 to 1016ns 32bit, 125MHz 32bit, 125MHz 8ns Steps NIM Gate Delay Scaler Scaler 0 to 1016ns 32bit, 125MHz 32bit, 125MHz 8ns Steps Width Delay dECL 4 to 64ns 0 to 508ns Trigger 4ns Steps 4ns to dECL TDC 16

# • EPICS driver implementation schemes

New firmware with additional scalers for EPICS

**FPGA Scalers** 

DAQ scalers FIFO 90 EPICS scalers FIFO 10

VME bus A24 160 Mbyte/s Via /dev/shm/vmeBus **EPICS** driver

Software FIFO < 200k

### New firmware with snapshots of scalers

**FPGA Scalers** 

DAQ scalers

Snapshot of DAQ Scalers updated By FPGA VME bus A24 160 Mbyte/s Via /dev/shm/vmeBus **EPICS** driver

Software FIFO < 200k