12GeV Trigger meeting notes:

16-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson

9-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, S. Kaneta, B. Moffit, H. Dong, E. Jastrzembski

24-Feb-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, S. Kaneta, B. Moffit, H. Dong

10-Feb-2012: C. Cuevas, W. Gu., A. Somov, Beni Z., J. Wilson, N. Nganga, B. Raydo, S. Kaneta

27-Jan-2012: C. Cuevas, W. Gu. B. Moffit, A. Somov, J. Wilson, N. Nganga, H. Dong, B. Raydo. S. Kaneta

20-Jan-2012: C. Cuevas, W. Gu. B. Moffit, Ed Jastrzembski, A. Somov, Beni Z., J. Wilson, N. Nganga,

13-Jan-2012: C. Cuevas, W. Gu. B. Moffit, N. Nganga, J. Wilson, S. Kaneta, Ed Jastrzembski, A. Somov

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0. Trigger/Clock/Sync – TI/TD

16-March-2012

4 proposals have been received with the final evaluations due next week by the tech review committee.

→TS initial testing:

Rear transition board is not assembled yet, but will be soon so testing with the GTP can begin soon. Firmware and new TS library development is in progress.

9 –Mar 2012

Bid schedule on track. Will need to evaluate proposals within 5 days.

TS prototype (1st article) is in the initial test stage, with plenty of firmware development in progress. BUSY circuits are being tested.

The global trigger consolidated crate idea will work and needs to be discussed with the Hall A and Hall C DAq folks.

PEPPo solution with the pipeline TI is solved. (Interrupt issue with TI) New firmware application for PEPPo (helicity integration mode) is ready for testing.

24-Feb-2012

The production TI-TD turnkey solicitation has been posted to the website and proposals should be received by 16-March-2012. So far the procurement is staying on schedule, and evaluations of proposals will be reviewed and completed within a week.

The prototype TS is presently in the initial functional test stage and William is progressing with test activities. At some point soon after the HPS test run priority has subsided, we can progress toward running the TS with the GTP, SD and SSP to verify the remaining L1 Trigger latencies.

Operation of the global trigger crate where a SSP, SD, and TI are the only boards required, has been reviewed by Chris and William. In Halls A & C, the DAq crates that will be included in the L1 Trigger total < 8, so in principle it makes sense to use only a TI in the supervisor mode. One could use a TS and TD, but the simple solution of a TI in supervisor mode should be adequate. We will need to evaluate the Hall A and C DAq plan and document their setup requirements.

10 Feb 2012
→TS board was sent for minor repair/rework, and is undergoing initial functional testing.
→The TI-TD bid package has been posted to the JSA vendor site. The bid evaluation team has been formed, and hopefully bid packages will arrive soon.
→The rear transition module that will interface the TS to the GTP lvpecl outputs has been designed. Fabrication, assembly and testing will become activities soon.
→Need to create a signal interface sketch that shows the consolidated global trigger crate proposal. As a reminder, this consolidation global crate feature would be very useful for Halls A & C because the total number of DAq crates is << 64. So, SSP, TD, SD, GTP, and TS would reside in this crate. No show stoppers, but careful review of the VXS signal map is needed.

27-Jan-2012
→Assembled TS prototype has been delivered and William will begin the initial inspection and testing.
→TI - TD procurement has started and the next step will be evaluating the bids from the vendors.
→A brief discussion regarding details about the signaling requirements for the consolidated Trigger Supervisor/Global Trigger crate idea proposed the first week of 2012. It would be a good idea to sketch the critical signals if SSP, GTP, SD, TD and TS all share the same crate. The trigger information is serialized to the SD→TD, so details of how this is handled needs to be identified.

20Jan2012
→TS 1st article is planned for delivery the week of 23-January. Initial testing will occupy at least a few weeks.
→TI –TD specification is complete and is going to be circulated for final signatures. Final quantities have been decided and the total production order is for 185 units.
Front panel and other peripheral hardware for the production TI-TD lot has been submitted to the procurement department.
→The TS rear transition board design is complete. William will wait for TS initial testing, then TS_Rear Transition board will be sent for manufacturing and assembly.

13Jan2012
-->TS 1st article board will be assembled and delivered in a few weeks. Acceptance test firmware in development.
-->TI-TD procurement has started and is approved. Accessory orders have been placed, and production quotes have not been received or evaluated yet. Accessory items are front panels, F/O Transceivers, and alignment pins.

Last week a discussion of consolidating the global crate to include SSP, GTP, SD, TD and TS was held and several issues have been identified. I believe there is an issue with the serial transmission of the trig1 and trig 2 signals from the TS to the SD, but other than that, this configuration should work.

1. *SUB-SYSTEM PROCESSOR (SSP)*

16 March 2012
Simulated CTP input data streams to reflect the HPS setup. More testing will be needed before installing in the hall.

24 Feb 2012
SSP will be used for the upcoming HPS test run. Ben has simulated the code required to handle the two crates that will be used to readout the two crates. Hardware testing of the new firmware is scheduled in about a week, and then the HPS hardware should be configured for the experiment.

10 Feb 2012
→Effectively the same report as last week. New updated Estimate-To-Completion (ETC) schedule shows the SSP in production before the end of fy12.

27-Jan-2012
→Same report as last week and Ben is prepared to begin the ECO details and start procurement as soon as other high priority activities are near completion. Production order would include quantities and spares for Hall D. Estimate To Completion schedule will be updated and forwarded to the relevant folks.
→The Heavy Photon Search group will begin a spring beam test run and Ben has started initial work for handling the data streams from two CTP. The SSP will manage the cluster finding trigger information from the new HPS EM Calorimeter configuration.

20-Jan-2012
SSP is effectively ready for production, so we can verify quantities and start the procurement (Hall D and B?). Ben's schedule shows other projects with higher priority, and the ECO list for the initial SSP is minor. Target June 1, 2012 as the procurement start date for the Hall D and B quantities.

13Jan2012
SSP "pre-production" could be advanced and initiated by summer if folks have a need for a few boards for evaluation/testing. There are a few groups that would like to use a SSP so maybe this makes sense. Minor circuit ECO will be completed before this pre-production run.

Final production order will be placed in August -2012 and will coincide with installation of crates and other infrastructure that will be needed before pre-commissioning can begin in the halls.

Development activity for the HPS test run in March-2012 will include firmware for the SSP, and a requirements document is in place for the new firmware required for the FADC250. This is a very aggressive schedule for the March run, but a goal has been set.

2. CUSTOMERS

16 March 2012
→Test and repair activities are progressing with the FADC250 that are not functioning at 100%. There are several issues and these modules do not pass the low level functional testing step.
Discussion to purchase Ethernet to JTAG interface so that any firmware downloads to the CTP can be performed remotely. Hall B funds will plan to purchase these items.
→PEPPo firmware development work is nearly complete and has been a significant effort! The future positron machine is close to reality!

24 Feb 2012
➔ We will need to locate (and repair?) as many FADC250 boards from the pre-production batch for use during the Hall B HPS experiment. Several boards will be used for other beam test setups, (see 10-Feb notes below) and a FADC250 test station is set up in EEL109 to facilitate the testing/repair.

→The PEPPo group has set their final requirements and Hai has completed the firmware code. Ed and Hai will test and deliver a FADC250 unit to them by the end of 5-March-2012.

10 Feb 2012
→Customers are abundant!
-Hall B -- HPS beam test (March -> May)
-Hall D – FCAL beam testing (ongoing)
-Hall D – BCAL beam testing (proposed for March)
-Injector – FADC250 firmware modifications

27-Jan-2012
→No new report, and we will have to locate the remaining working FADC250 to populate the 2nd crate for the HPS beam test.

20 Jan 2012
→Jeff briefly reports on the visit to ACDI. May receive 1st article production boards by end of February! Good news overall.
→The HPS spring run is a high priority given the 6GeV beam will turn off in May. New firmware for the FADC250, CTP and SSP are in progress. The HPS spring run will require at least two VXS crates and twenty six FADC250 boards. Hall B presently has 16 FADC250 boards that are connected the original Inner Calorimeter.
→Make a decision/directive to declare the experiment plan(s) for beam testing AND HPS. Repair and gather up FADC250 to meet the HPS and other beam test needs.

13Jan2012
-->The production order for FADC250 has been awarded and the production orders for the SD and TI-TD boards is in procurement waiting for bids. We have started discussions with the Accelerator group and MIS to use a common database tool to manage the volume of different DAq boards that will be used in all of the halls. This tool is a work in progress, but will handle all equipment tracking and repair information.

3. "B" Switch - Signal Distribution Module (SD)

16 March 2012
Five proposals received with one not truly acceptable. Evaluation summary will be submitted to procurement next week.
→HPS installation and test will take higher priority than the SD acceptance test procedure.
→As soon as the procedure is at a final draft, one of the technicians should perform the procedure from scratch.

9 March 2012
Proposals are due today, with 5 days of evaluation.
Acceptance test procedures in place and ready for production boards. 10 1st article boards.
Initial test procedure will be executed in EEL109 next week by one of the techs to see if the procedure is reasonable or requires modifications. Front panel PRs are complete.

24 Feb 2012
SD production procurement has been ratified, and posted to the public solicitation page. Turnkey companies have up until 9-March-2012 to submit proposals and we can begin the evaluations within a week after the receipt of the proposals.

Nick has been working on the refinement of the acceptance test plan and the final procedure should be evaluated by a few technicians to verify the procedure steps.

10 Feb 2012
→Has the PR for ALL peripheral hardware been sent for approvals?
→Production bid evaluation team has been selected. Production bid package not released to the JSA vendor page yet.

→Continue the acceptance test development and finalize procedure documentation.

27-Jan-2012
→Create PR for ALL peripheral hardware components needed for the production SD modules. The account codes used for the SD board PR will be used in the appropriate percentage to purchase these items.
→Update the acceptance test procedure to a final draft format and it would be a good idea to run through the procedure to verify the duration and accuracy of the test.

20-JAN-2012
→Nick has completed the purchase requisition, specification and all account managers have approved and signed the requisition. The total production order is 124 SD units. The orders for the peripheral hardware (front panel, alignment keys, other?) will need to be submitted soon using the same account allocations.
→Update the ETC schedule for production boards.

13-JAN 2012
→Signature approvals for the production order is 50%.
PRs for accessory items needs to be submitted. Accessory items are front panel, and alignment keys. This PR can use the same account codes and quantity breakdown.
→Nick has created a test plan document, and will need to modify and update this test procedure in preparation for the 1st article production test acceptance and production unit testing.

4. System Diagrams/Fiber Optics

16 March 2012
Brad S. (Hall C) suggested a simple MTP Fiber test in hall c using a few of the short jumper cables. The suggestion is to simply place a fiber patch cable in Hall C for the remainder of the 6GeV experiment and then test the fiber cable to see if there is any transmission problem. Setting up an 'active' test would take some effort with hardware/software using an evaluation board and the 150m fiber. This way a measurement of fiber degradation over a finite time interval with a known dose rate could be achieved. Ben, Chris, Brad.

10 Feb 2012
No update

27-JAN-2012
The final lengths of the trunk cables will be known AFTER the cable trays and other platforms are installed in the Halls. These trunk cables are the most expensive part of the system and the peripheral components E.g. (Patch panels, patch cables) can be purchased as soon as a purchase requisition is issued.

13JAN2012
Peripheral components can be purchased now for the trigger fiber optic system. For example, the patch panels and patch cords can be purchased. The trunk fiber cable will not be purchased until the cable trays and platforms are in place, so that an accurate length can be given to the selected vendor. Looking at the schedule, these length values for the trunk cables will be ready by summer 2012.

December 2011
No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

5. Two Crate DAq test configuration

16 March 2011
→Some discussion about the full crate testing and presently we do not have enough modules to proceed with this effort. We will need to have a draft procedure soon, and will also need a 'standard' CPU setup for the full crate tests.

9 March 2012
Legal and illegal register ranges, etc. New library developments for latest trigger modules in progress.

24 Feb 2012
One VXS crate will remain the EEL109 test rack, and before the end of summer the goal is to operate and measure the total latency and performance of the global trigger modules running in unison. There will be CODA libraries needed, and firmware for the SSP, SD, TS, and GTP should be at a stable (initial) version to begin these tests.

10 Feb 2012
No new updates, and part of the reason the test station has been quite is that the modules have been deployed! Will need to prepare for global trigger module testing soon though.

27-JAN-2012
No new updates.

20-JAN-2012
→We had a discussion on testing the production front end "payload" boards in a full DAq crate with all the trigger boards. Clear agreement that this testing will be essential before delivering a full crate to the Hall location.
→A few bullet points on the procedure to test a full crate of "payload" boards. (FADC250)

Prerequisites

- Each board will have passed individual acceptance testing
  - FADC250, SD, CTP, TI as examples all have individual acceptance test procedures.
- Final firmware revision will be loaded into payload modules
- VXS crate will be load tested and prepared for new modules
- Single board computer (ROC) will be configured with proper OS and pre-tested
- Required function generator, oscilloscope, and test cables will be available.
- Tests:
  - Deterministic timing alignment: Synchronous "Playback" mode.
  - Asynchronous "Playback" mode with Trig_2 generated with random pulser.
  - Inject pulse signal to 16 input channels and verify trigger generation and readout of input signals. 16 of 256 channels is 6.25% occupancy. Low, but probably useful. Could ramp up the pulse rate to test trigger rate.
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13-Jan-2012
-->Chris will draft a "Full DAq Crate Test Procedure" document. The idea is that all boards in a single crate will have passed individual acceptance testing and these boards will need to be operated in concert with CODA and together in a VXS backplane to verify full readout and synchronization testing. This will eliminated full crate troubleshooting in the halls.
-->Random pulse generator testing with playback data needs to be documented.
-->Need to get started with configuration and test goals for the global trigger crate testing. We will have ALL custom trigger boards in either production or 1st article format by March, and can begin testing the SSP, GTP, SD, TD and TS in a full crate. Needless to say, significant CODA driver library development activities will increase.

3 June 2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16 July 2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

16 March 2012
Still a few bugs with the transfer of PCAD files to Altium. Merging power nets seem to not work properly.
ECO list is complete and new options are strongly considered and will be designed. E.g. PPT17 (Cpu slot) can run PCIExpress.

9 March 2012
Files have been transferred to Altium. Problems! Need to get the Altium experts involved. Start ECO and set a schedule to get the board to production by July.

Plug but no play. A few issues with trying to run new HPS FADC250 and CTP code. Alignment testing and then cluster finding!

HPS group has sent simulation data to Ben. Ben is working on integrating this data into a full simulation of the FADC250 → CTP → SSP.

24 Feb 2012
→Scott reports that the new firmware development for the CTP that will be used for the upcoming HPS spring test run is converging. It appears that the new cluster finding code will fit including the gigabit transceiver blocks and the fiber transceiver blocks.
Functional simulation (system level) testing will begin next week. A small scale (3-4 FADC250 ,CTP and SSP) hardware test will need to be completed also before deploying this hardware in the hall.
→The beginning of implementing the ECO required for the production CTP has started with Jeff and Hai reviewing the ECO and also checking notes for any new I/O that has been requested since the original requirement document(specification) was created. Goal is to have the CTP in production before end of summer.

10 Feb 2012
→Full steam ahead on the new cluster finding algorithm firmware for the CTP(s) that will be used in the upcoming HPS test. The requirements and description document have been updated. Hopefully there is ample time to thoroughly run test verification for the new firmware before operations begin in the hall.
→Jeff and Hai have started the ECO for the production CTP boards.

27-Jan-2012
Scott presented initial results of his cluster finding algorithm firmware for the HPS trigger application. Additional meetings with the HPS group will be required and the initial requirements have been discussed. Scott will continue to develop the firmware and iterations will be needed to be sure the algorithm runs at full speed and does not exceed the FPGA resources.

20-Jan-2012
→No report from Hai, BUT, Scott is presently working on custom firmware for the HPS cluster finding trigger algorithm. The calorimeter mapping and other information is starting to take shape, and Scott could implement the firmware in both a CTP (Xilinx) or GTP (Altera). The HPS

beam test configuration will require two VXS crates to fully instrument their calorimeter and the new cluster finding trigger algorithm will be implemented and tested.
Due March 1.
→Lets not forget that the CTP production order will need to be started this summer. As described last week, the Hall D units in principle could be ordered by the summer. Will require time to modify existing circuit board design for final production version.

13-Jan-2012
Discussion about how to proceed with the FY12 order of production boards for Hall D. Existing version meets(exceeds?) requirement for energy summing and other parameters. Goal is to order production units by 1-Aug-2012.

Will continue to work with the CLAS12 folks for a written requirement document to justify a new design for the CTP. The new requirements for the CTP may in fact affect the design of the SSP, so this will have to be discussed in detail. Schedule impact will be a significant issue to consider.

7. GTP and Global Crate Developments

16 March 2012
→Scott has made significant progress with the HPS cluster finding firmware development and at some point soon all the components, (FADC250, TI, SD, CTPs and SSP) will have to be operated together. Hardware testing has started using simulation files to generate the input signals that will verify the new firmware (code). The schedule is still aggressive and by April the hardware will need to be assembled in Hall B.

10 Feb 2012
Same report as 27-Jan-2012
27-JAN-2012
→GTP Ethernet firmware development has been dominated by the HPS firmware development work for now.

20-Jan-2012
→Scott has taken on the activity to develop the HPS cluster finding trigger using the CTP and possibly the GTP to process the modified serial streams from each of the sixteen FADC250 payload boards that will be connected to the Hall B Inner Calorimeter(IC). LOTS of development and testing in a short time, but this will take a priority over some of the other activities needed for the GTP.
→Need to shift the production order for the GTP to the latter part of FY12 because it makes sense and there are several essential and critical tests that need to be completed with the global trigger boards (SSP, TS, TD) before ordering the production boards for ALL halls. The quantities for the TS and GTP are low (<10) and there is time before pre-commissioning begins in the halls.

13-Jan-2012
-->Scott continues to make progress on the Ethernet development, and will complete testing of the FO transceiver soon. Some work activity will be completed by Scott for the upcoming HPS run and we also discussed activities to verify the limits of the FADC250 to CTP Gigabit serial speed. (Works at 2.5Gb/s but hardware limits need to be tested @5Gb/s). Scott can use a FADC250 and the GTP to document results of the higher speed transfer.

***ACTION ITEMS*: Next meeting -Friday 23 March@ 10AM in F226**