12GeV Trigger meeting notes:

16-Sept 2011: C. Cuevas, B. Moffit, S. Kaneta, W. Gu. A. Somov, N. Nganga, E. Jastrzembski

9-Sept 2011: C. Cuevas, B. Moffit, S. Kaneta, W. Gu. A. Somov, H. Dong, N. Nganga, E. Jastrzembski

2-Sept 2011: C. Cuevas, B Moffit, B. Raydo; J. Wilson, S. Kaneta, H. Dong, W. Gu. D. Abbott, A. Somov

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0. Trigger/Clock/Sync – TI/TD

16-Sept-2011
→Two of the latest versions of the TI boards are in the EEL109 test station.
→Register changes on the latest boards will need to be addressed with software changes and the timing of the fiber skew adjustment to align both crates in the system needs to be completed.
→Plan for TS "design review" the week of 26-Sept and William will organize the meeting.

9 Sept 2011
→It is time to replace the existing TI boards(older revision) in the EEL109 lab with the latest revision. The 10 new TI boards have been tested and updated to match the latest CODA library. The latest TI boards will be installed in the EEL109 two crate test stand the week of 12-Sept.
→William has the TS schematics and other design files complete and it is a good time to organize a 'review' meeting with the appropriate engineers for circuit design analysis and discussion. William will set up this meeting soon.

2 Sept 2011
→All ten boards are tested and working. It appears that the LGA voltage regulators were repaired.
→Install one pre-production TI (Version 4, Rev2) board in the EEL109 test stand.
→Discussion regarding firmware selection by software. Example, TI 'Master' function or normal TI function. Can firmware be all inclusive and then the modes are selectable? Capability of writing FPGA configuration device via VME exists also.
->Review configuration circuitry/requirements before FINAL order. Minor ECO will be required.

These functions appear to work correctly. William will continue testing all functions of the TI in Trigger Distribution mode... The firmware will be different for TI and TD, so there will have to be a library 'driver' for these different boards.

1. SUB-SYSTEM PROCESSOR (SSP)

16 Sept-2011
No report
9 Sept 2011
No report. SSP is presently being used in the two crate test station and performs well.

2. CUSTOMERS

16-Sept 2011
→VME FADC250 control and fan-out boards will be fabricated and assembled to support the detector groups. Most detector groups will use only a few FADC250 boards and will not need the SD for these small tests.
→ **Keep as many FADC250-V2 boards in EEL-109 lab to finish two crate testing!**

9 Sept 2011
→Delivery of FADC250V2 boards to the following groups:
Injector group: 2 modules(A. Camsonne)
Hall D: 1 modules (A. Somov)
Hall B: 1 modules (S. Boyarinov)

→Need to consider the proposed setups for the beam tests coming up in Oct/Nov. How do these setups need to be configured. SD? Front panel clocks/synch/trigger? CTP?

3. *"B" Switch - Signal Distribution Module (SD)*

16 Sept 2011
→ All six pre-production boards have been tested for hardware functionality.
→ Two out of six boards pass all functionality tests. Two pre-production SD modules will be installed in the EEL/109 two crate test station.
→ SNR test data has been collected. Very complete data analysis presentation presented by Nick.

9 Sept 2011
→All the boards will be tested for hardware functionality. All boards have front panels, and the Tyco Gigabit backplane connectors have been installed.
→ Nick continues to test SNR using a single FADC250. Some noise floor issues still remain to be solved to be able to present data. May be able to extend raw data window to allow for more points in a sample window, which would allow an FFT of many more points (lower frequency analysis)

4. *System Diagrams/Fiber Optics*

No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

5. Two Crate DAq test configuration

16-Sept 2011

→CTP #4 (FX70T) has been tested with sixteen FADC250 and will be inserted in the EEL109 test station today. The second CTP (LX110T) will be tested next and moved to the EEL109 when completed.
→The CTP firmware will need modification to complete the request from D. Abbott and B. Moffitt regarding the mapping of the VME slots to show Busy status, enable/disable Gigabit lanes, and control of token passing.

9-Sept 2011
→The two crate testing has been slowed down this past week because 16 FADC250 are needed to test/verify the CTP firmware. Bryan reports that the driver library has been finalized for the version of FADC250 boards that have been distributed.
→Ed reports that the 2eSST readout mode testing with the latest software shows a few issues. Will need to be investigated and any firmware changes can be downloaded to modules in situ.
→Bryan showed a few plots of data from the "Playback" mode and there are a few issues/questions because the data results show some sort of offset that should not be present when using the "Playback" setup data. Hai will have to investigate the "Playback" mode to see where the problem may occur.

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➔ The following is a copy of the test goal list created several months ago:

- **Goals of the integration testing:**
- **-Verify clock distribution through TID->SD and measure jitter to front end boards**
- **-Verify trigger rate and readout rate for a variety of occupancy levels.**
- **-Verity token passing scheme**
- **-Verify CTP operation with sixteen FADC250 @2.5Gbps**
- **-Test playback mode feature on two crates and verify operation with SSP.**
- **-Measure and record overall trigger latency. (Could include SSP)**
- **-Verify full 2eSST readout from payload modules**
- **-Verify TI-D features and use one TI-D in TS 'mode'**
- **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**

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3 June 2011

→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

22 April 2011

The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
See older note dates for the list.

6. Crate Trigger Processor (CTP)

16-Sept-2011

→See notes in the two crate test section.

9-Sept-2011

→Hai has a breakthrough with sixteen FADC250V2 boards passing trigger data to the CTP in one crate. Only two errors in 6 hours with sixteen FADC250V2 boards!!!! A new JLAB record! The errors are in the final sum value, and the errors do not crash the system. So far these tests only include the FADC250V2 and CTP board.
→Move one of the CTP to the EEL109 today, and setup/test the 2nd CTP early next week.
The EEL109 test station will have one CTP with a V5LX110 and one CTP with a V5FX70T.
→Plan to populate both crates in the EEL109 lab by end of next week.

2-Sept-2011

-->15 FADC250V2 boards with the CTP are under test in the DAQ lab.
→This test will need to be re-tested with ALL FADC250V2 AND CTP clocked by a single source.
→CTP#4 with 'FX70T are being tested now with the 15 FADC250V2
→By end of next week 9-Sept we will have two CTP in the EEL109 test station!

7. GTP and Global Crate Developments

16-Sept-2011

→DDR2 memory testing is completed at full clock rate of chips.
→Initial testing of all 4 Densi-shield output ports with cable and termination board
→Ethernet interface work still progressing.
→Initial discussions on how the GTP will be programmed to interface to the experiment trigger requirements. Probably need to have a few specific meetings to get these ideas on paper.

9-Sept-2011

→Ethernet and DDR2 memory testing is a work in progress and is going well.
→Nios core etc is on a trial basis. Will cost some money for a license.
→5Gb/s for two lanes from one SSP board has been successfully tested. Proves the Xilinx to Altera marriage will work. (Aurora protocol PRSB31 testing)
→Densi-shield cable testing may be next goal
→Paper/Poster work is in progress for ICALEPS-2011

2-Sept-2011

→Configuration bits loaded to the device and are stored on the board.
→MGT transceivers have been tested on slot 13 @5Gb/s PRBS-31 signal pattern; SSP was used so Xilinx to Altera marriage produces no known problems.

- ➔ DC power test matches expectations, no heat sink needed at this time. May need to be considered for final board.
- ➔ Memory testing DDR2, and other hardware testing is progressing nicely
- ➔ Densishield testing, Ethernet testing,

ACTION ITEMS: Next meeting -Friday 23 Sept @ 10AM in F226