Trigger meeting notes:

23 Jan 09: C. Cuevas, A. Gupta, H. Dong, E. Jastrzembski, F. Barbosa, J. Wilson, M. Taylor

16 Jan 09: B. Raydo, C. Cuevas, A. Gupta, H. Dong, A. Somov, E. Jastrzembski

12 Dec 08: B. Raydo, C. Cuevas, A. Gupta, H. Dong, J. Wilson, F. Barbosa

Updated prototype board status table:--23 Jan 2009

Quantity	Description	Location	STATUS
7	**10bit FADC250**	**EEL109/DAQ Lab**	**Trigger testing**
1	**10bit FADC250**	**EEL109**	**In Repair**
1	**12bit FADC250**	**Indiana University**	**FCAL testing**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Trigger testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Initial functional testing**
1	**Crate Trigger Processor**	**Send for assembly as soon as parts received**	**Send 9 Feb 2009**
2	**Signal Distribution**	**Receive from board house on 21 Jan**	**Ship to assembler on 29Jan09**

0. Trigger/Clock/Sync – TI/TD

23 Jan 2008

No report and the TI modules are functioning without problems and the latest firmware has been stable since installation about a month ago.

Sebouh has returned to school and is at a point where he can demonstrate his work on the GUI and interface code that will be used to control the Signal Distribution card and the CTP card. His application will read/write data to the Trigger_Interface module with the Wiener USB-VME controller. His I^2C firmware will be used on the Atmel microcontroller which bridges the information from VME to the two I^2C devices. (SD and CTP).

12 DEC 2008

No update and Sebouh will continue this work when he returns for school.

1. FIRMWARE TESTING

23 JAN 2009

→The firmware for the FADC250 modules has been stable for many months, including the updates to the TI module.

→We discussed the effort required to develop and test the Source Synchronous Transfer (SST) mode to achieve higher VME data transfer rates. Ed described the two edge VME transfer mode and associated handshaking requirements, and explained that it makes more sense to put full development effort into the SST method because the readout controllers(ROC) support this SST method. This development effort will take a higher priority because we need to test the data readout rates in combination with the specified 200 KHz trigger rate.

→Hai explained that the present firmware will sustain 165 KHz trigger rate using the “Q” readout mode. Optimization of the firmware will develop as soon as we begin the production design.

16 JAN 2009
No problems to report and the new readout parameters have been added to Ben's test stand data displays and records.

Hai has completed the development of the firmware download procedure that describes the method to reconfigure and download the FADC250 FPGA from VME. The discussion that followed focused on the method to verify that the new firmware download was successful. This download procedure will be refined, and the main point is that Hai has developed the code that manages the transfer of the new firmware via VME to the Xilinx Eproms.

2. *FADC250 Control board (SD-FP == Signal Distribution – Front Panel)*

23 JAN 2009
These are complete.

3. CUSTOMERS

23 JAN 2009
→Collaboration meeting for GlueX starting 29 Jan and it would be a good opportunity to discuss details of the results from the FCAL group at IU. Schedule priority is still focused on the CTP testing, but code development plans for implementing the algorithm in the FPGA for the timing readout can begin.

→There is a group at Oak Ridge National Lab that has an interest in implementing the FADC250 design for their Accelerator upgrade projects. Since ORNL is a DOE lab it should be easy to exchange the design with them, and to request funding from them when we are prepared with the next revision of the board for production quantities.

16 JAN 2009

No new progress to report. Hai has focused his time on the CTP testing.

Alex Somov had a few questions about the ability to readout raw data AND 'Q' value from each channel for every trigger event. This may be a method used during commissioning to verify the 'Q' mode function that is performed in the Fpga. Other system level trigger questions were discussed and it is clear that further discussion is needed to document/clarify overall trigger system requirements/functions.

12 DEC 2008
Hai has started researching methods to implement the function that was presented by the group at IU. The FCAL IU group has the 12 bit FADC250 module and have performed offline analysis with the data gathered from their detector setup. The Sqrt (ln(x)) function produces timing resolution of less than a nanosecond, and Hai has investigated the use of a CORDIC algorithm for use in the Fpga. Further implementation will develop.

4 "B" Switch - Signal Distribution Module (SD)

23 JAN 2009
The three bare boards have been received and look fine. Abhishek and Mark will begin testing the bard board for any defects and send these boards with the parts to the assembler. Schedule to ship on 29Jan09 and we paid for a seven day delivery.

As soon as the assembled SD boards are received there are plenty of preliminary functional tests to perform and these test results will be documented on Abhishek's test plan. Soon after, the SD will be installed in the full 20 slot crate and critical testing of the signal fan-out will begin.

16 JAN 2009

Abhishek presented his latest Altera functional timing verification for the FPGA that will control the Clock, Trigger, Sync, Busy and Token passing signals. He has successfully synthesized the firmware, and has instantiated the block of code that was developed by Sebouh Paul that will manage the serial control interface to/from the Trigger Interface module.

The SD boards will be shipped on 21 January, and two boards will be sent to the assembly company by next week (26Jan09). The assembly process is at least a week, and then Abhishek can begin the initial test plan for the SD board. Soon after, the SD board will be used to distribute signals in a full VXS crate and plenty of other tests can be performed.

There was a discussion about how to handle "half" crates that may be installed on experiments. In a 12 slot VXS crate, the payload slot that would normally have the Trigger Interface module does not exist.(PP18) This means that the SD and CTP would have to receive the global clock/sync/trigger signals from a front panel module. For Hall D, I believe we have specified full 20 slot VXS crates for all the detector readout systems, so this should not be an issue.

In cases where a VXS "half" crate is used, the CTP will have to receive the common signals (CLK,Trigger,Sync) from the front panel. This detail will have to be discussed further and implemented on the final board design.

5. System Diagrams & Test Stand Activities

23 JAN 2009

→No report since Ben was out this week. Results from recent measurements in the test stand will be presented at the Hall D Collaboration meeting.

→Many more tests are planned once the CTP and SD boards are ready to be installed in the test stand crates.

→A new RF switch has been purchased and will be controlled with a FlexIO module. This switch will allow us to connect each input on the FADC250 module to a single signal source. The present pulse source is an Agilent arbitrary waveform generator, but in principle, the signal source could be a PMT.

→The Wiener 21 slot VXS backplane will be installed in one of the test stand crates on 4 Feb 2009. The other crate will retain the Elma 20 slot VXS backplane and we can verify that the new Wiener design meets specifications.

16 JAN 2009

As a quick review, the following tests have been completed with the FADC250 boards, TI/TD, and front panel signal distribution boards:

- ✓ Test LX25 with high rate trigger pulse train on all inputs simultaneously
- ✓ "System" clock jitter with fiber distribution and existing front panel signal distribution boards. These tests will need to be repeated once the SD module is ready.
- ✓ Signal to Noise Ratio (SNR) Plenty of test data, and the results so far will establish the baseline SNR value. These tests should be performed with multiple channels per board, and with multiple boards transferring VME data and with all the Gigabit links active to measure differences from the baseline results. VME data transfers are not dual edge yet, but testing SNR with higher the higher bus rates will be important
- ✓ 10 bit FADC250 charge mode Vs 12 bit charge integrating ADC(LeCroy 1182) Ben presented the initial results from the test, and further details will be presented at the Hall D collaboration meeting.

GUI and data display software will continue to be developed by Ben for the upcoming CTP and SD test stand activities.

- Real Time Conference 2009 – Beijing, China 10-15 May, 2009
  Dave Abbott proposed that abstracts be created for submission and that the 12GeV trigger system offers an abundant source of topics to present at the conference. The overall Trigger/DAQ system could be the main presentation, and the poster sessions could present details of new results from the CTP and SD crate tests. Abstract submission deadline is 20Feb2009

6. Crate Trigger Processor (CTP)

23 JAN 2009
Loopback testing is underway for the initial CTP module. The heat sink material has been ordered and the material will need to be machined to fit properly on the CTP board. The heat sink will cover all three FPGA will provide adequate cooling for the Virtex5 parts when the full code is running all SerDes lanes. We cannot activate all 16 payload slots, but we can certainly test the CTP with up to 8 FADC250 modules.

16 JAN 2009
Functional testing with the first module is going well. A heat sink will be added to cover the three large Fpga on the module. Hai will follow his test plan for the initial functional testing and then begin the testing with multiple FADC250 modules in a crate. Discussions about how to use the CTP output data were presented, and since we will not have a SSP module for awhile, we could implement the testing of the CTP fiber optic output data stream with a Xilinx evaluation board. We may not be able to fully implement the 4 lanes of fiber optic data, but the final CTP sum data can be tested.

12 DEC 2008
The power section tests for the initial module passed and the results have been recorded on Hai's test document. Clock circuitry was populated also on this power section test board, and since no problems were identified, the entire assembly kit was sent to the assembler. The fully assembled CTP will be at JLAB on 5 Jan 2009.

The initial test document for the CTP has been drafted and there are numerous tests to perform before establishing the gigabit links with the FADC250 payload modules.

ACTION ITEMS: Next meeting will be Friday 30 January 2009 → CCF228 @10am
*Hall D Collaboration ongoing, but we will still plan to meet.