

## **12GeV Trigger meeting notes:**

23-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson, E. Jastrzembski, Beni Z.

16-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson

9-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, S. Kaneta, B. Moffit, H. Dong, E. Jastrzembski

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### **0. Trigger/Clock/Sync – TI/TD**

#### **23-March-2012**

Vendor source evaluations are due to William for the TID production units. By next Monday the summary report will be sent to Kathleen.

TS manual in progress and no other test results presented. Rear transition board has been assembled and will be tested with the GTP soon.

#### **16-March-2012**

4 proposals have been received with the final evaluations due next week by the tech review committee.

→TS initial testing:

Rear transition board is not assembled yet, but will be soon so testing with the GTP can begin soon. Firmware and new TS library development is in progress.

#### **9 –Mar 2012**

Bid schedule on track. Will need to evaluate proposals within 5 days.

TS prototype (1<sup>st</sup> article) is in the initial test stage, with plenty of firmware development in progress. BUSY circuits are being tested.

The global trigger consolidated crate idea will work and needs to be discussed with the Hall A and Hall C DAQ folks.

PEPPo solution with the pipeline TI is solved. (Interrupt issue with TI) New firmware application for PEPPo (helicity integration mode) is ready for testing.

### **1. SUB-SYSTEM PROCESSOR (SSP)**

#### **23-March-2012**

Ben has requested changes to the CTP-FADC250 code. No show stoppers seen, but lots of work to complete before installation and use on the HPS experiment.

Production SSP work has not been started, but minor ECO and any other changes will need to be completed before production order is placed.

#### **16 March 2012**

Simulated CTP input data streams to reflect the HPS setup. More testing will be needed before installing in the hall.

## **2. CUSTOMERS**

### **23-March-2012**

→PEPPo FADC250 board has been repaired and is ready for final test. Deliver by 26-March.  
→HPS

- At least 9 more FADC250 modules have been located and will need to be tested. There are still issues with the units that have been tested, and so far none of the boards pass the test 100%.

→Hall D – FCAL beam testing (ongoing)

→Hall D – BCAL beam testing (proposed for April)

→Hall D – Pair Spectrometer will use several FADC250 boards

### **16 March 2012**

→Test and repair activities are progressing with the FADC250 that are not functioning at 100%. There are several issues and these modules do not pass the low level functional testing step. Discussion to purchase Ethernet to JTAG interface so that any firmware downloads to the CTP can be performed remotely. Hall B funds will plan to purchase these items.

→PEPPo firmware development work is nearly complete and has been a significant effort! The future positron machine is close to reality!

→Customers are abundant!

-Hall B -- HPS beam test (March -> May)

-Injector – FADC250 firmware modifications

## **3. “B” Switch - Signal Distribution Module (SD)**

### **23-March-2012**

→SD production board fabrication and assembly bids have been evaluated and summary sent to procurement. The prices for the production quantities have been revealed to the source selection committee. No final decision yet, but the award will be ratified soon.

→Acceptance test plan discussion was very useful and insightful. In the end, we will plan on using 16 of the production FADC250 modules to fully verify the proper operation of each production SD module. Using 16 fully tested FADC250 boards in the SD acceptance test procedure will eliminate the need for the test operator to cycle the crate power and change the location of the payload test board. Great discussion and Nick will have to modify his existing test procedure.

### **16 March 2012**

Five proposals received with one not truly acceptable. Evaluation summary will be submitted to procurement next week.

→HPS installation and test will take higher priority than the SD acceptance test procedure.

→As soon as the procedure is at a final draft, one of the technicians should perform the procedure from scratch.

### **9 March 2012**

Proposals are due today, with 5 days of evaluation.

Acceptance test procedures in place and ready for production boards. 10 1<sup>st</sup> article boards.

Initial test procedure will be executed in EEL109 next week by one of the techs to see if the procedure is reasonable or requires modifications. Front panel PRs are complete.

## 4. System Diagrams/Fiber Optics

### 16 March 2012

Brad S. (Hall C) suggested a simple MTP Fiber test in hall c using a few of the short jumper cables. The suggestion is to simply place a fiber patch cable in Hall C for the remainder of the 6GeV experiment and then test the fiber cable to see if there is any transmission problem. Setting up an 'active' test would take some effort with hardware/software using an evaluation board and the 150m fiber. This way a measurement of fiber degradation over a finite time interval with a known dose rate could be achieved. Ben, Chris, Brad.

## 5. Two Crate DAq test configuration

### 23-March-2012

Same report as last week and a few discussions regarding the details of the procedure have been exchanged. (Bryan – Chris) There has been discussion about setting up multiple locations to test full DAq crates, and there will be several types of full DAq crates tests to develop.

### 16 March 2011

→Some discussion about the full crate testing and presently we do not have enough modules to proceed with this effort. We will need to have a draft procedure soon, and will also need a 'standard' CPU setup for the full crate tests.

### 9 March 2012

Legal and illegal register ranges, etc. New library developments for latest trigger modules in progress.

### 24 Feb 2012

One VXS crate will remain the EEL109 test rack, and before the end of summer the goal is to operate and measure the total latency and performance of the global trigger modules running in unison. There will be CODA libraries needed, and firmware for the SSP, SD, TS, and GTP should be at a stable (initial) version to begin these tests.

### 20-JAN-2012

→We had a discussion on testing the production front end "payload" boards in a full DAq crate with all the trigger boards. Clear agreement that this testing will be essential before delivering a full crate to the Hall location.

→A few bullet points on the procedure to test a full crate of "payload" boards. (FADC250)

#### Prerequisites

- Each board will have passed individual acceptance testing
  - FADC250, SD, CTP, TI as examples all have individual acceptance test procedures.
- Final firmware revision will be loaded into payload modules
- VXS crate will be load tested and prepared for new modules
- Single board computer (ROC) will be configured with proper OS and pre-tested
- Required function generator, oscilloscope, and test cables will be available.
- Tests:
  - Deterministic timing alignment: Synchronous "Playback" mode.
  - Asynchronous "Playback" mode with Trig\_2 generated with random pulser.
  - Inject pulse signal to 16 input channels and verify trigger generation and readout of input signals. 16 of 256 channels is 6.25% occupancy. Low, but probably useful. Could ramp up the pulse rate to test trigger rate.
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### **3 June 2011**

→ **Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!**

**16 July 2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.**

## **6. Crate Trigger Processor (CTP)**

### **23-March-2012**

→ Need to revisit the schedule for the production CTP activity. There are still a few problems with the transfer of the CAD files from (old) PCAD to (new) Altium. Existing ECO will take highest priority over any new design feature! There was a brief discussion to consider the inclusion of a high speed Gigabit serial link to the CPU slot (PP-17), but there is not a great deal of time before the production lot must be ordered for the Hall D needs.

→ During the discussion of the SD acceptance testing, it is clear that we can use the same idea for the acceptance testing of the CTP production units. In other words, use 16 fully tested FADC250 boards for the critical testing of the CTP production units.

### **16 March 2012**

Still a few bugs with the transfer of PCAD files to Altium. Merging power nets seem to not work properly.

ECO list is complete and new options are strongly considered and will be designed. E.g. PPT17 (Cpu slot) can run PCIExpress.

### **9 March 2012**

Files have been transferred to Altium. Problems! Need to get the Altium experts involved. Start ECO and set a schedule to get the board to production by July.

Plug but no play. A few issues with trying to run new HPS FADC250 and CTP code. Alignment testing and then cluster finding!

HPS group has sent simulation data to Ben. Ben is working on integrating this data into a full simulation of the FADC250 → CTP → SSP.

### **24 Feb 2012**

→ Scott reports that the new firmware development for the CTP that will be used for the upcoming HPS spring test run is converging. It appears that the new cluster finding code will fit including the gigabit transceiver blocks and the fiber transceiver blocks.

Functional simulation (system level) testing will begin next week. A small scale (3-4 FADC250 ,CTP and SSP) hardware test will need to be completed also before deploying this hardware in the hall.

→ The beginning of implementing the ECO required for the production CTP has started with Jeff and Hai reviewing the ECO and also checking notes for any new I/O that has been requested since the original requirement document (specification) was created. Goal is to have the CTP in production before end of summer.

## **7. GTP and Global Crate Developments**

### **23-March-2012**

→ HPS cluster finding code for the CTP has a few issues to work through. No show stoppers, meets timing, firmware changes, progress is still moving forward, ISE 13.2.

→ Testing the dedicated cable link outputs with the TS prototype will need to be completed soon, but take a lower priority than the HPS activities.

### **16 March 2012**

→Scott has made significant progress with the HPS cluster finding firmware development and at some point soon all the components, (FADC250, TI, SD, CTPs and SSP) will have to be operated together. Hardware testing has started using simulation files to generate the input signals that will verify the new firmware (code). The schedule is still aggressive and by April the hardware will need to be assembled in Hall B.

**ACTION ITEMS: Next meeting -Friday 30 March@ 10AM in F226**