12GeV Trigger meeting notes:

22 Oct 2010: C. Cuevas, H. Dong, A. Somov, N. Nganga, W. Gu, , B. Raydo, E. Jastrzembski, S. Kaneta

1 Oct 2010: C. Cuevas, H. Dong, A. Somov, N. Nganga, W. Gu, B. Moffitt, B. Raydo, E. Jastrzembski, S. Kaneta

24 Sept 2010: C. Cuevas, H. Dong, A. Somov, N. Nganga, W. Gu, D. Abbott, J. Wilson, B. Moffitt, B. Raydo, E. Jastrzembski, S. Kaneta

17Sept2010 – No meeting →BIA Review
10Sept2010 – No meeting →Hall D Collaboration
3 Sept 2010: C. Cuevas, H. Dong, A. Somov, N. Nganga, W. Gu, J. Wilson, B. Moffitt, B. Raydo, E. Jastrzembski, S. Kaneta

Updated prototype board status table:--22-October 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 >>>>>>>>>** **SN002 >>>>>>>>>** **SN003 >>>>>>>>>** **SN004 >>>>>>>>>** **SN005 >>>>>>>>>** **SN006 >>>>>>>>>** **SN007 >>>>>>>>>** **SN008 >>>>>>>>>**	 **DUKE** **DUKE** **Injector Group** **EEL – 126** **Hai's office** **F-Wing Lab** **Hall A** **EEL – 126**	 **B. Sawatzky** **B. Sawatzky** **J. Grames** **FDC test setup** **Needs repair** **F117 (A. Somov)** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded Sent to IU for FCAL testing** **12Oct2009** **'64x crate and LinuX Cpu sent 24Jan10**
4	**Trigger Interface** **Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**F-Wing F110**	**CODA Library development**
1	**Crate Trigger Processor**	**F-Wing(Hai)**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**F-Wing F110**	**CODA Library development**

0. Trigger/Clock/Sync – TI/TD

22 October 2010

William reports that the TI-D testing is progressing and that the VME section has not been fully tested yet. The firmware development for the VME section includes a remote download feature to load the FPGA boot prom and this testing continues. The EEprom (Fpga configuration device) has been removed from at least one of the boards, and the pads were damaged. For now the FPGA can be programmed via the JTAG port.

The fan-out module that was designed for the CAEN V1290 high resolution TDC has been partially assembled and passes initial testing. The initial fan-out board has not been tested with a TDC yet, and 6 boards will be sent to for assembly. The front panel design has been completed, and once the fully assembled board has been received it can be tested with the TI-D and TDC for full qualification.

We had a discussion about plans for the Trigger Supervisor (TS) and William mentioned the use of a different fiber optic interface. It was not clear what this fiber interface would be used

for, and we also discussed the number and style of I/O that needs to be on the front panel of the TS. William has a draft specification that should be reviewed soon by all.

1 October 2010

TID testing is progressing and fiber transceivers have been tested in loop back mode. The firmware development has started and the initial testing with a VME interface is progressing. There have been minor revisions to the two initial prototype boards and integrated testing with other modules in the crate are planned for fy11

The V1290TDC fan-out module will be tested and was partially assembled by Jeff and Armen. Test results will be distributed soon, and any minor revisions will need to be corrected before production and operation with the CAEN high resolution TDC

3 September 2010

The fan-out board for the V1290TDC has been received and will be partially assembled soon. The mezzanine card has been received and has been assembled for testing with the TI-D board.

TI-D board testing is progressing and the status was reported at the recent Hall D collaboration meeting. Firmware development will become a higher priority as soon as the hardware has been tested.

Armen and Jeff have assembled several new VME front panel clock-trigger-sync modules to support FADC250 boards that have been distributed to other groups. Ed has verified the operation of the boards.

1. FIRMWARE TESTING

22 October 2010

Not exactly a firmware discussion point here, but no further discussion about using a common VME 'Broadcast" addressing scheme to manage common module commands has taken place. I believe this would be a valuable time saving method for common commands, and can be handled in the FPGA.

We have determined that there will be a single GTP in switch slot A of the global trigger crate, so the backplane mapping can remain the same as a front-end crate. The SSP will have to be modified, but the pair mapping is a minor revision. This will restore the token passing to the SSP and eliminate the signal fan-out requirement for the GTP.

1 October 2010

Discussion about a common VME "Broadcast" address space to manage commands that are common to all modules on the bus was discussed. The private token passing scheme is still planned for all VXS style modules, and only token in-out were implemented on P2 for the latest revision of the FADC250.

We revisited the pair mapping diagrams for the front end modules and noted that NO token passing lines were included for the global trigger crate. Some form of token passing can be achieved by using status bits from the SSP (payload boards) to the TID.

VME – SST firmware has been completed and will be thoroughly tested on the SSP and FADC250 revision as soon as the modules are received.

The dedicated pair from TID to SD will need to be completely defined soon as firmware for both modules will be needed as soon as the SD revision has been received and assembled.

3 September 2010

→The SSP functional testing is progressing and please see notes from 20-Aug. Testing with CTP continues and verification of serial lanes to the GTP will obviously be delayed, but should not stop production of the SSP.

→New definitions for the I^2C control and monitoring have been proposed by William and discussed at several meetings. The new PLL devices on the SD will be controlled through the SD Fpga and the SD Fpga will interface to the TI-D through I^2C. A dedicated pair between the SD and TI-D was added for this revision, and the method of data transport will need to be finalized by William and Nick.

2. *SUB-SYSTEM PROCESSOR (SSP)*

22 October 2010

Ben reports that the SSP has been repaired and has been sent back to Jlab. He will continue testing the SSP and can continue to fully check all functions. (SODIMM – DDR2, etc). The module will need to be tested with the TI-D, and of course the SD board to verify the initial global trigger crate 'system'. We can also use the existing CTP in another crate to record and test data transfer from two CTP to a single SSP.

1 October 2010

Ben has tested virtually all functions of the SSP with the exception of the SDRAM and output serial streams to the GTP. The board has been sent to the assembler for reflow/repair of one of the FPGA that appears to have solder connectivity problems. Fiber transceivers have been exercised and BitErrorRate(BER) testing has been measured to be well within limits.

3 September 2010

Test results with the SSP prototype was presented at the Hall D collaboration. The board has not been sent back to the assembler for reflow yet, and testing with a single CTP continues.

3. CUSTOMERS

22 October 2010

Brad Sawatsky has borrowed to FADC250 modules for an experiment at Duke U. These boards are configured with the 'standard' firmware and not the Moeller firmware. The units are on a short loan, and will be returned within a few months.

1 October 2010

Plans for integration testing are taking shape for FY11 and will include all the latest board revisions for the FADC250, SD, TID, CTP and SSP. The new VXS and VME64x crate order has been awarded and we should begin receiving these crates by December.

3 September 2010

I can report here that a decent number of "pre-production" FADC250 units will be here by December and the detector groups (Hall D and Hall B) need these for various test purposes.. The VXS 1st article crates will arrive by December as well and the crates will need to be load tested and at least 2 payload modules will be needed to verify the VXS backplane map.

Plans for a multiple crate test with the full "suite" of trigger modules have been drafted as FY11 work plans and will require plenty of coordination. Test goals will need to be established so that it is clear that all the boards work in unison and meet or exceed design specifications.

4 "B" Switch - Signal Distribution Module (SD)

22 October 2010

The boards have been received and visually inspected. They look very good and will be sent to the assembler on Monday 25-Oct for a 5 day assembly period. The front panel has been completed, and Mark will send this for fabrication soon. The initial test period for the SC-Rev1 board will begin in a few weeks. Nick will spend more time with firmware development as time permits.

1 October 2010

Nick reports that the board is ready for a thorough review of the manufacturing files before ordering and the front panel work has started too. The initial cost estimates to build eight(8) bare boards has been received and is a reasonable price. The estimates for assembly will be sent the week of 4-Oct and the parts will need to be kitted soon.

Nick has performed a HyperLynx BoardSim analysis of the latest layout and does not report any anomalies for the present board layout and board layer stack up.

3 September 2010

→The components have been placed and routed and minor changes have been made to the placement of the DC-DC converter and other regulators. Nick has managed to complete these changes and soon the board will be ready to check before manufacturing files are sent.

→Components have been received for up to eight SD units, and it is not too soon to send out for assembly quotes.

5. System Diagrams & Test Stand Activities

22 October 2010

No update

3 September 2010

No update

20 August 2010

No new updates reported. The topics of pedestal subtraction and multiple triggers will continue to be discussed and at some point soon, final specifications need to be spelled out so that firmware changes can be started.

16 July 2010

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

   The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

   Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within

the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

Crate Trigger Processor (CTP)

22 October 2010

Two CTP are at the assembler and are due to be completed by 11-Nov. Testing the CTP can begin as soon as they are received. Recall that at least one of the CTP will have the faster grade parts and will be tested at 5Gbps in conjunction with the FADC250-V2 modules. Plenty of test activities will begin once we receive these boards.

1 October 2010

The assembly house has the two CTP and no issues are reported with the assembly kit, but the silkscreen-bottom layer will need to be updated once Jeff returns.

We have a few weeks until the assembled boards are received, and we should meet with Sergey B. to discuss implementation plans that will be needed IF the experiment for Sept-11 is approved.

3 September 2010

→Jeff has sent the assembly kit for two more CTP and delivery will be approximately 2 weeks. Scott will help Hai with the initial testing of these additional CTP and prepare them for testing with multiple FADC250 boards.

6. Projects for FY11 (GTP and Global Crate Developments)

22 October 2010

We have had several good discussions about the GTP and have reviewed requirements for Hall D and a proposal by Hall B to support more than one GTP. Present design plans include support of up to 8 SSP by a single GTP. So, 64 front end Level 1 crates can be supported, which easily satisfies Hall D for instance. More SSP can be supported but the additional payload port slots must be wired on the GTP. We will definitely support an Ethernet connection to the GTP and it is not clear if we implement an Ethernet pair from PP17 considering the CPU candidates may not have the P0 interface.

The GTP prototype will be a very close cousin to the CTP and will not have to support the fan-out features of the SD board (Switch-B). The pair mapping sketch for the global trigger crate will be updated to show the details and will effectively be a replica of the front end crate map.

Scott has learned the Altium tools and will begin with test board designs that will be used to test the new version of the FADC250 and to support testing of the CTP and SD boards. These boards are straightforward designs and offer very good practical experience. Soon after the schematics for the GTP prototype will be committed.

1 October 2010

GTP progress pace will improve significantly and Scott has started some research for implementing more than eight(8) SSP in the global trigger crate using cross point switches. We have to clearly understand the signal mapping already established for the TID and SSP, and also clearly take into consideration the duplicate function of the GTP in the B-Switch slot as the Signal Distribution functions cannot be omitted.

ACTION ITEMS: **Next meeting → Friday 29 OCT 2010 at 10AM in F228**