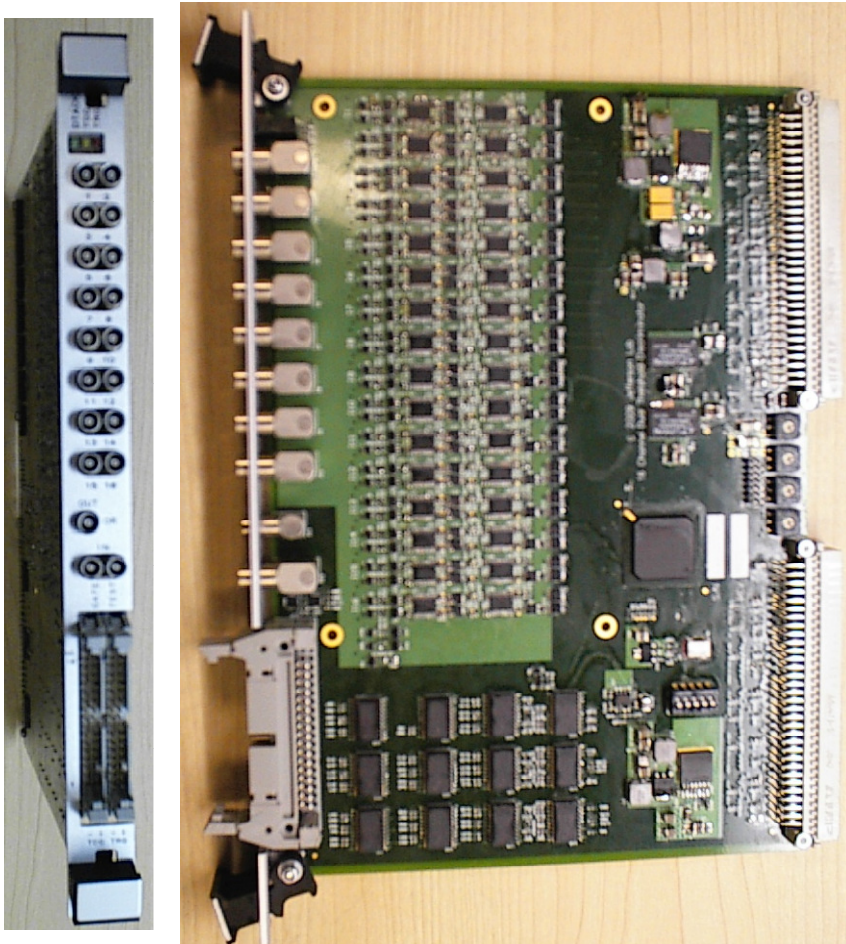


JLab Discriminator Status

Benjamin Raydo

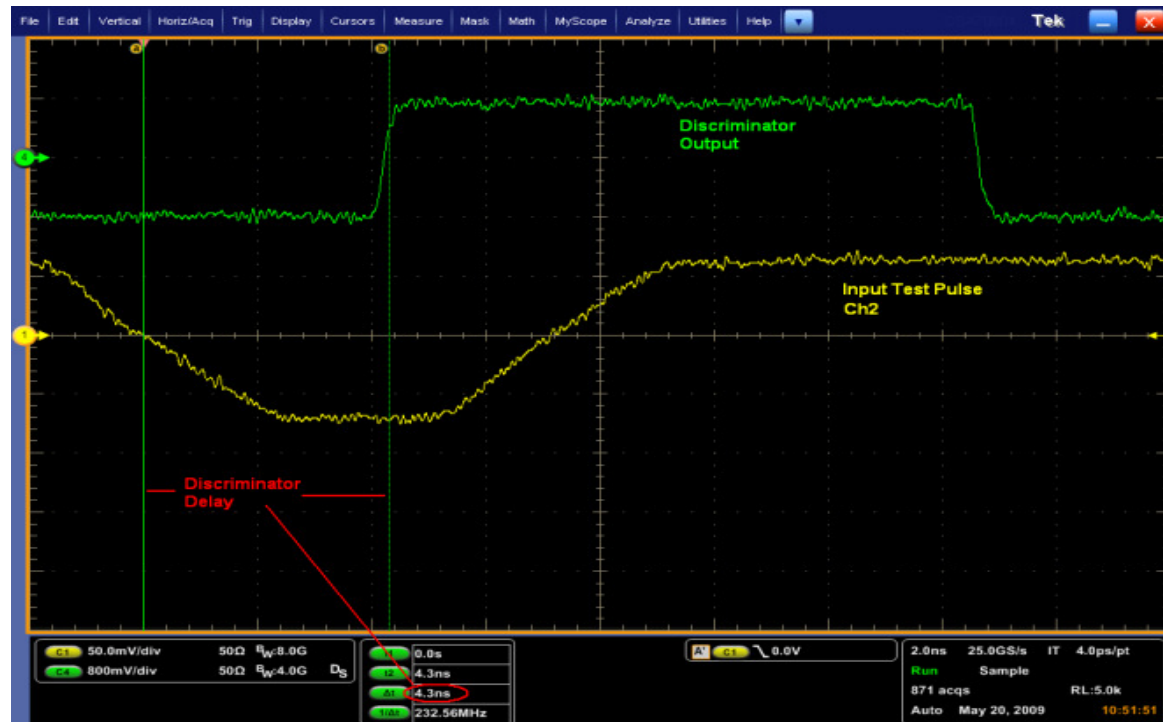
Jan 6, 2010

Discriminator Prototype



- 16 Channel Discriminator working prototype
- Dual-threshold (0 to -1V, 1mV steps)
- Non-updating mode
- Scalers are kept for both thresholds
- Standard VME interface (A32/A24, D64 support)

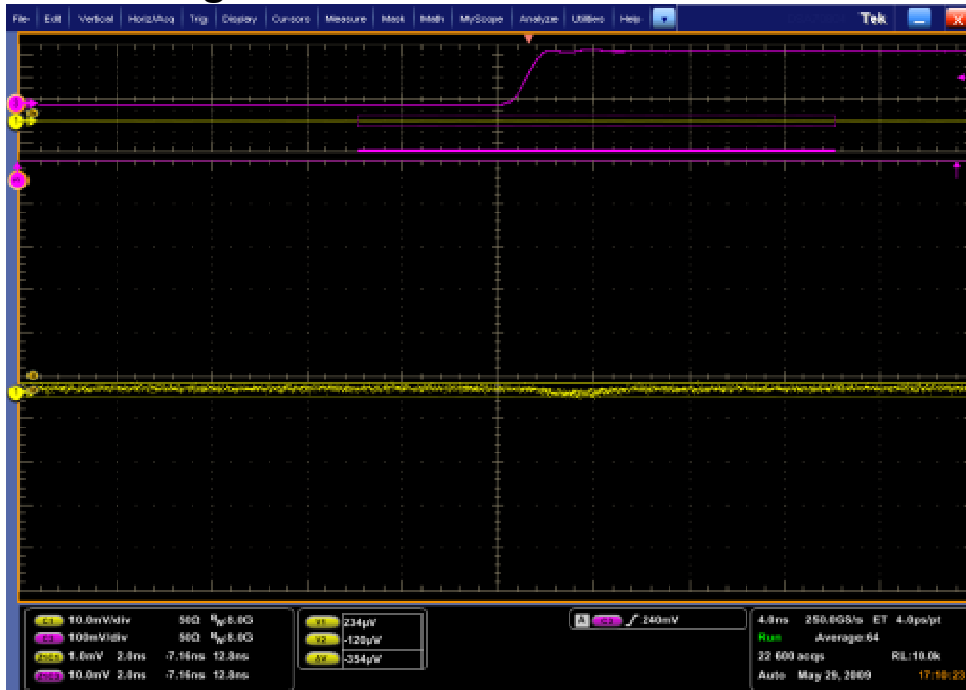
Input-to-Output Delay



Fast response time $\sim 4.3\text{ns}$

Channel-to-Channel Isolation

JLab Design:



CAEN V895:

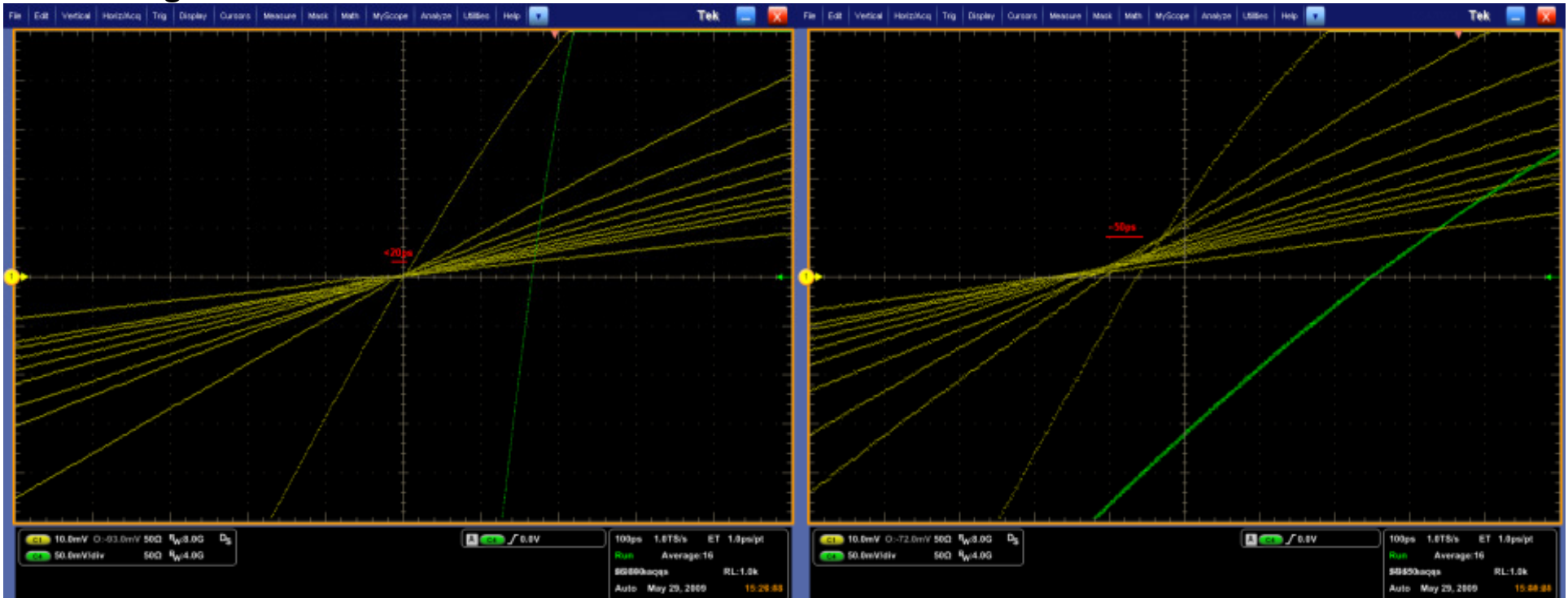


- 1V/ns, 500mV step used on adjacent test channel. Victim channel shown in yellow.
- Note scales: JLab 1mV/div, V895 10mV/div
- JLab design provides very high channel isolation (design uses shielded Lemo connectors)

Slew Rate Dispersion

JLab Design:

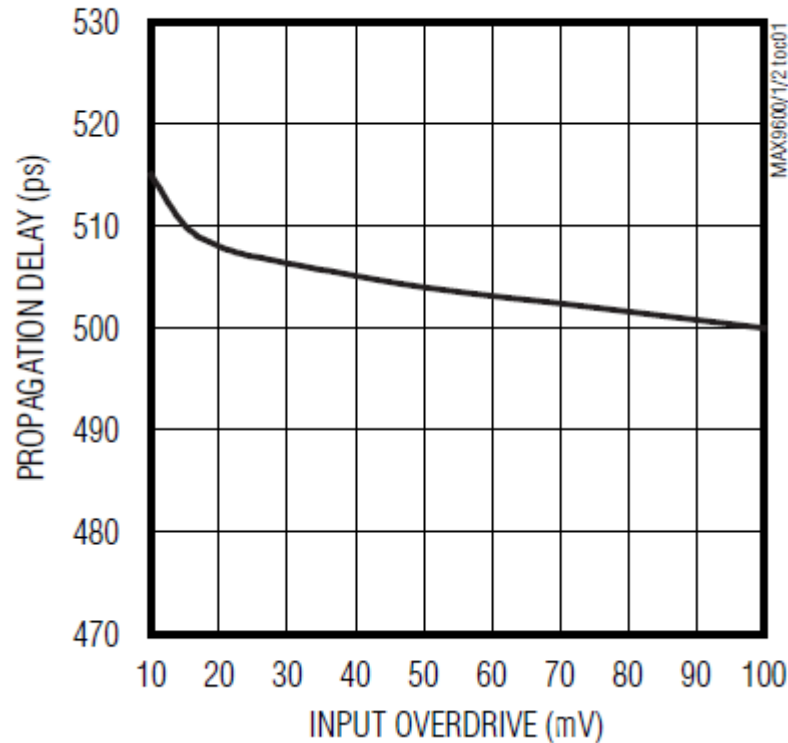
CAEN V895:



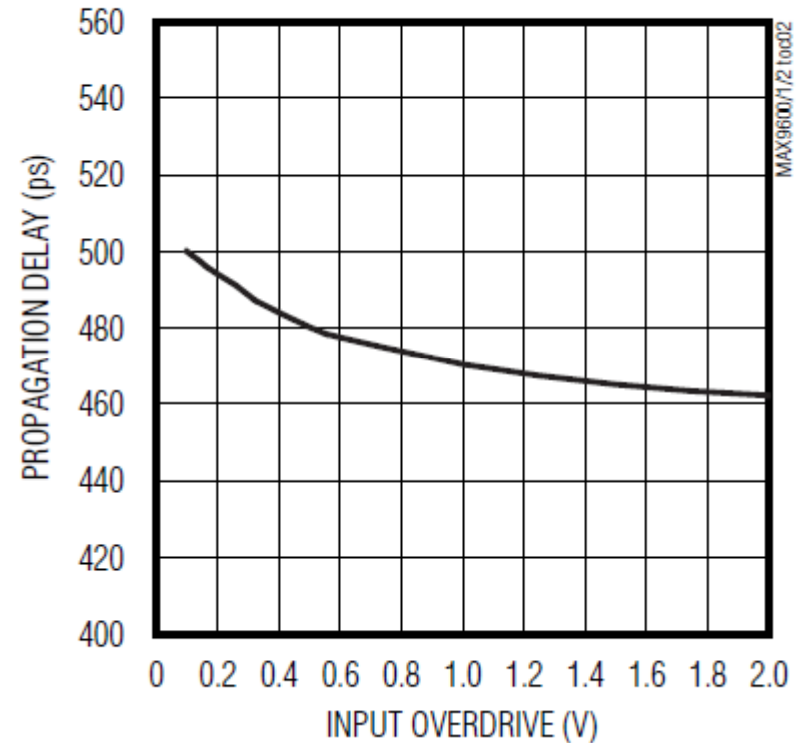
- Slew rates varied from 20mV/ns to 250mV/ns, 100mV overdrive pulse
- Green trace shown is the discriminator output used as scope trigger
- Ideally the yellow traces would intersect at the same point
- Measured dispersion: JLab $\sim 20\text{ps}$, V895 $\sim 50\text{ps}$

Overdrive Dispersion

PROPAGATION DELAY vs. INPUT OVERDRIVE
($V_{CC} = 10\text{mV TO } 100\text{mV}$)



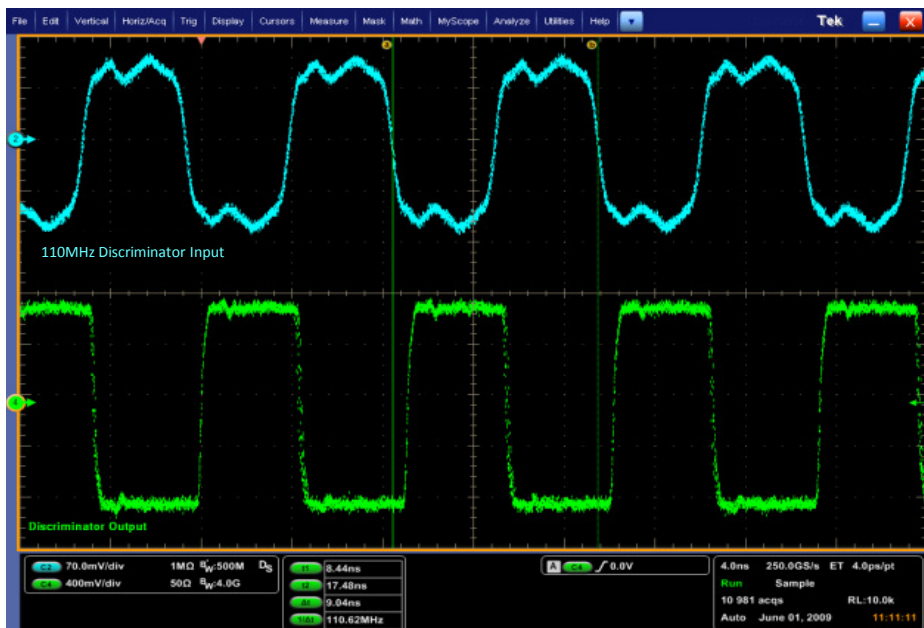
PROPAGATION DELAY vs. INPUT OVERDRIVE
($V_{OD} = 0.1\text{V TO } 2\text{V}$)



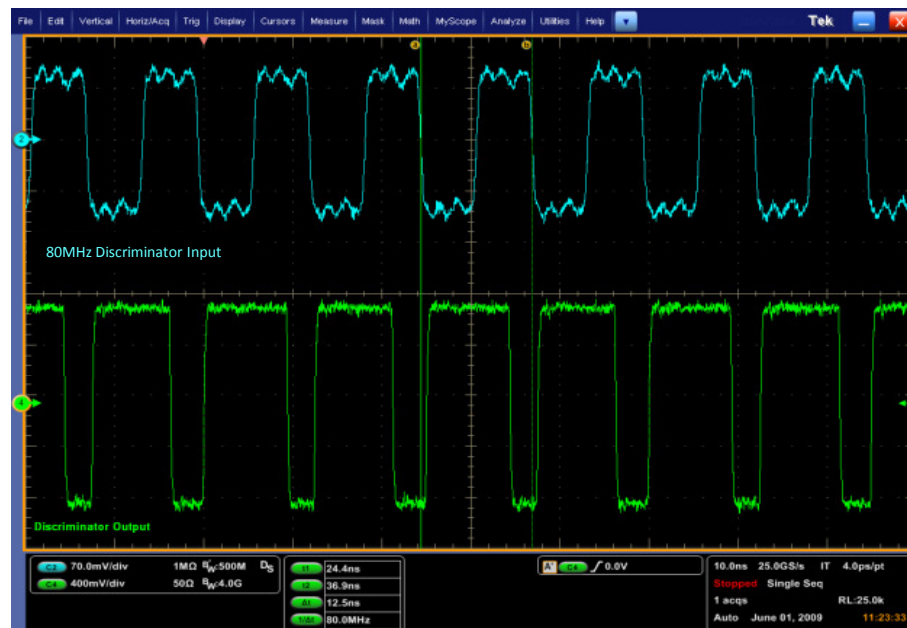
- Overdrive dispersion has not been measured – will be done with new test jig
- Overdrive dispersion graphs taken from comparator datasheet (2V/ns rise time signal)

Maximum Rate

110MHz rate w/4ns output pulse width:

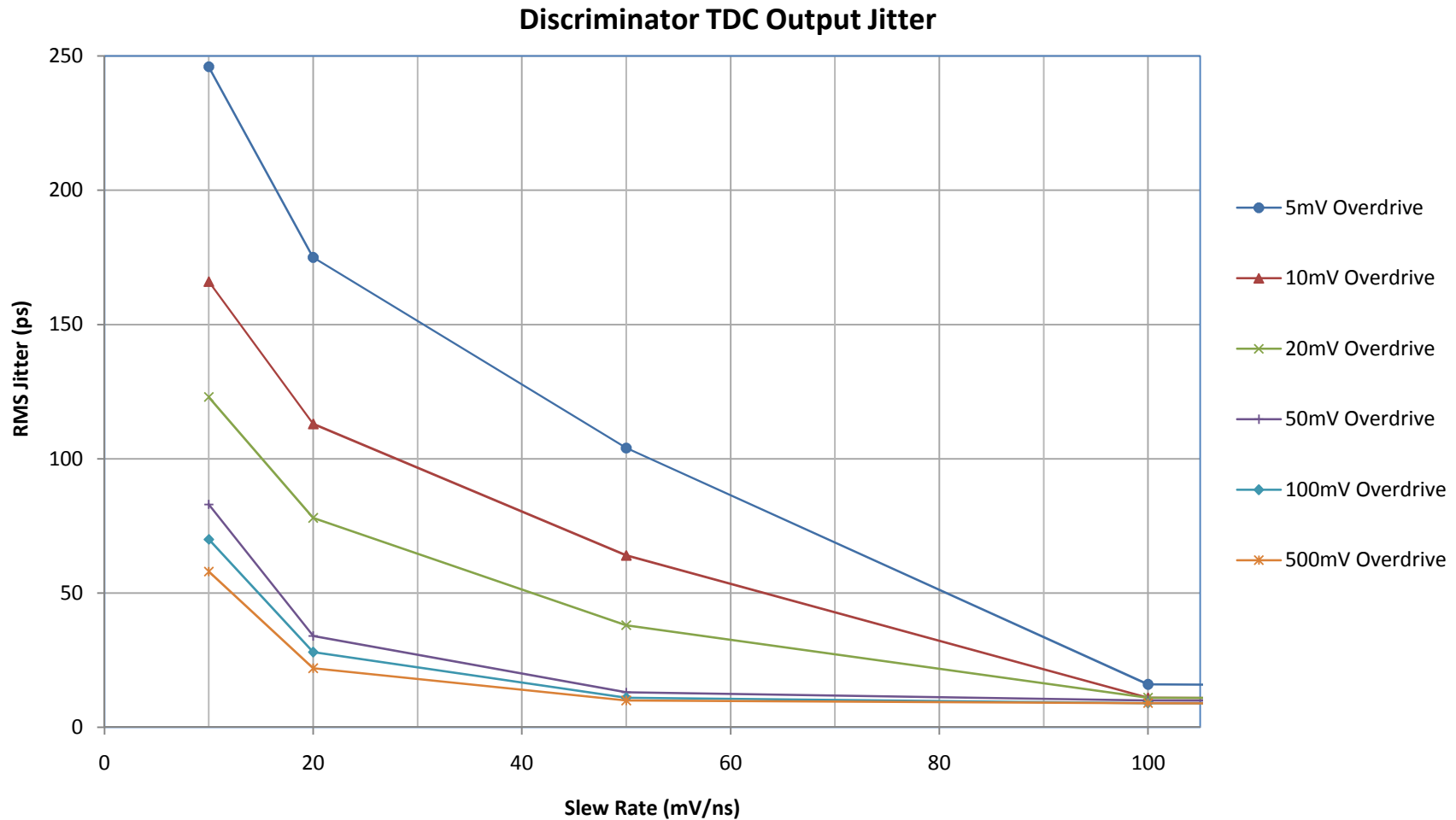


80MHz rate w/8ns output pulse width:



- Pulse width effects double pulse resolution (discriminator operates in non-updating mode)
- TDCs will require minimum input pulse width (F1 – 4ns?)

Jitter Performance



- Greater overdrive and/or slew rate improves jitter performance
- 1MHz variable slew rate/amplitude square wave used for test

Next Steps

- Revision of the prototype is almost complete (several changes for cleanup & optimization, main discriminator characteristics will not change)
- Small order of 5 boards for Hall B, 2 for Hall D will be underway this month. Will confirm schedule once build package is received by assembler.
- Pedro Toledo from University of Chile has arrived for a 6 month period. He will be responsible for building an automated test rig that will verify functionality and critical performance characteristics of production boards.