12GeV Trigger meeting notes:

19 Feb 2010: C. Cuevas, H. Dong, J. Gu, E. Jastrzembski, B. Raydo, J. Wilson, A. Somov

5 Feb 2010: C. Cuevas, H. Dong, J. Gu, J. Wilson, E. Jastrzembski, B. Raydo, A. Somov

22 Jan 2010: C. Cuevas, H. Dong, J. Gu, J. Wilson, E. Jastrzemski, B. Raydo, A. Somov

15 Jan 2010: C. Cuevas, H. Dong, J. Gu, A. Somov, J. Wilson

8 Jan 2010: C. Cuevas, H. Dong, J. Gu, A. Somov, J. Wilson

Updated prototype board status table:--19 February 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Daq Lab F110** **EEL – 126** **EEL109** **F-Wing Lab** **Hall A** **EEL – 126**	 **Test Board** **OK Hall A Student** **Moller Spare** **FDC test setup** **Needs repair** **F117 (A. Somov)** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded** **Sent to IU for FCAL testing** **12Oct2009** **'64x crate and LinuX Cpu sent 24Jan10**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Testing complete**

0. Trigger/Clock/Sync – TI/TD

19 February 2010

No schedule updates and the topic of discussion was focused on the fiber optic transceivers. William pointed out about a month ago that the Avago makes another transceiver rated at 2.7Gbps that is about $100 less than the 3.25Gbps version that we are planning to use.

In the production quantities for both Halls B & D the $100 savings per part could save $34K See table below

Board Quantity	Board	Per board multiplier	Total		
12	SSP	8	96		
60	CTP	1	60		
84	TI	1	84		
12	TD	8	96		
			336	@$500	$168K
			336	@$400	$134K
				Saving	$34K

The vendor should be able to provide a few samples of the 2.7Gbps units for testing. One of the arguments is that the savings does not account for extra engineering time needed for thorough test evaluation of jitter and other performance requirements. If the vendor has trouble delivering the 2.7Gpbs parts soon, it may be moot.

5 February 2010

No updates to the schedule and William continues to make progress on the TI design activities.

A brief discussion about the assignment of the extra transmit and receive fibers from the TI to the TDs was started by Chris and the consensus was to connect these unused Tx and Rx pairs from the fiber transceivers to pairs on the FPGA. These signals will not require Gigabit resources from the FPGA, but by using the Select I/O features, these unused transceivers could be used as an additional data path between the front end crates and the trigger supervisor crate.

22 January 2010

FastTrack schedule has been created to show the activities associated with the design of the latest Trigger_Interface-Trigger_Distribution module. There are two other peripheral modules that are listed in the activity schedule and they are part of the TI development and also include fanout of the TI signals to the CAEN V1290 TDC.

8 January 2010

Progress on the new TI/TD module was reported by William. The schematic work and initial component placement have started, and there will be details to resolve for the mechanical placement of a mezzanine board that will be used if a TI/TD board needs to be used in a legacy system.

William updated the status of the distribution module that will be needed for the Hall B CAEN 1290 TDC units. These TDC do not use VXS, so a distribution module has been specified and the design is progressing nicely. Up to 16 V1290 units will be connected to the distribution module. This distribution module will receive the clock, trigger, and synch signal from the TI via P2.

William, Ed and Chris met 'offline' to discuss the activity and preliminary schedule for the TI/TD project and Chris will generate a FastTrack schedule and add this project to the overall Trigger System schedule.

1. FIRMWARE TESTING

19February 2010

Ed reports significant progress and plan to test on an existing FADC soon. Ben could also use the new VHDL code to on the new VME 16channel discriminator/scaler module. At some point in the not too distant future, Girard may be able to use the latest source code to implement the readout into the FADC125.

5 February 2010

Ed reports that the firmware development to transfer AHDL to a full VHDL source is progressing. The new firmware will need simulation verification and then there are a number of modules that can use the new firmware for field testing.

There was some discussion about the 12bit FADC250 board testing and that the FCAL group has achieved and presented results at the latest GlueX collaboration meeting. The plot that Matt Sheppard presented is included at the end of these notes. The algorithm that was implemented appears to work nicely and achieves the desired timing resolution. (See the plot)
The tests were performed using the local on board clock including the jitter from the clock distribution circuits.

22January 2010

Ed has been working on firmware development and transferring his VME SST readout code from Altera HDL (AHDL) to Standard VHDL that will be used on future designs. This code change will allow the firmware to be used on virtually any FPGA and not solely for Altera devices. Progress is going well and at some point soon, the latest VHDL version will be tested and verified.

8 January 2010

No new firmware issues have been reported and Ed has been busy with converting the VME SST firmware from Altera 'HDL" to standard VHDL. This new VHDL version will need to be verified and will be used on virtually all new VXS payload modules.

There will be a number of firmware activities started once the SSP prototype module is assembled later this year, and William will also join in the development of firmware for the TI/TD units.

2. *SUB-SYSTEM PROCESSOR (SSP)*

19 February 2010

Ben reported that other activities are taking a higher priority than the final routing of the SSP module. Ben has received the quotation for the two fiber optic transceiver models and we are waiting to see if the vendor can deliver two units for evaluation purposes.

Ben reviewed and requested that the pair mapping for the global trigger crate be changed to support the existing SSP design. The new pair mapping for the global trigger crate is on the M:drive.

5 February 2010

The SSP board is ready to begin the routing phase and Ben will be optimizing the DO files and other necessary parameters for the Specctra router. Starting soon after the routing phase, we should process an order for the components and take any advantage of lowering cost by consolidating common components orders for the TI-TD boards as well. The tentative plan is to order one fully assembled SSP.

22January 2010

Progress is ahead of the planned schedule and we talked about ordering components that show list a long delivery. We may be able to combine orders now for the fiber transceivers needed for the SSP and possibly the TI/TD prototypes. It is still too soon to create a final bill of materials.

The next stage of the board design is configuring and optimizing the auto-router. There will be plenty of time for post layout verification before ordering the bare boards. The 16 channel discriminator module has taken a higher priority for now, but soon enough the SSP will become the highest priority.

January 2010

The schematics for the SSP have been closely reviewed by Ben and Chris and the board placement activity is complete. This board is ready for routing and any long lead components should be purchased as soon as possible. The test plan for the SSP should also be drafted soon, and there are several trigger applications that have been proposed by the CLAS12 folks that will need to be reviewed before developing new firmware. The Hall D requirements for the SSP have been declared and reviewed, and give a firm starting point to test the performance of the SSP functions.

3. CUSTOMERS

19February2010

→Sasha has started using one of the FADC250 boards and has set up a test crate in the Fwing 1st floor lab. Dave Abbott has located a spare FADC250 unit which can be sent to Paul Eugenio in Florida. (GlueX TOF testing) Paul has modified a '64x crate so that the P0 connector on the flash board will not get damaged. Chris will check with Paul to see what other peripheral boards Paul may need to get going. The firmware will need to be updated and verified before sending the board. (Hai)

→Dave Abbott exchanged a GE Fanuc CPU with another model for the FCAL folks at IU. The new unit will be used by Girard Visser for continued testing with the new FADC125.

5 February 2010

→No new issues with the 12bit FADC @ IU. The number of working channels is fine for their testing purposes and I believe they have the new crate and Cpu working.

→Alex will receive a single FADC250 along with a small test crate, Cpu and VME-TI so that he can become familiar with the hardware and prepare a 'framework' that will interface simulation data(signals) to the front end FPGA. The data(signals) will be loaded into the front end modules and the trigger system can be tested using the simulated data(signals). Using this method, individual detector systems could be tested and verified using data that is effectively generated from each input channel.

→A single crate and FADC250 has been reserved for the injector group and they have submitted a letter of intent(LOI) for a new Compton Polarimeter system. The LOI lists the goals of the new apparatus and they are projecting a very high trigger rate and understand the triggering features and data acquisition modes of the FADC250. The request is not presently a high priority, but we should be able to set them up with the hardware when they are ready.

22 January 2010

We had a short discussion about the recent problems with several channels of the 12bit FADC250 module. Hai is convinced that the problem is associated with the tight setup & hold timing specifications for the Maxim 12bit part. There is little margin, and these timing issues may be creeping up because of temperature fluctuation. We do not believe we have seen these types of issues at Jlab with this unit, and the number of channels that are working are enough for the FCaL group to use for testing.

8 January 2010

→VME64x mini crate and new GE Fanuc CPU have been shipped to IU. The FCAL group has been using the VXS crate that was loaned to Gerard and Gerard needs the crate to finish testing the FDC flash modules. There has been recent work and a few troubleshooting questions from the IU folks when using the latest 12 bit FADC250, and hopefully these issues will be resolved without having to send the unit back to Jlab for testing. Looking forward to the results from the timing extraction algorithm!

→The Hall C folks have not stopped by to pick up the test crate and FADC250 module yet. I will ask them one more time and then see what other group could use the module. I have a request from the Accelerator Injector group so we will see.

→No recent news from the Moller folks in Hall A. I believe they are on track to use the module for Prex coming up in March.

4 "B" Switch - Signal Distribution Module (SD)

5 February 2010

No new activities planned and modifications to the existing modules will have to take place before testing begins with the latest version of the FADC250 boards and the SSP.

8 January 2010

The SD module will need to be revised to reflect the changes to the signal pair mapping for the front end crates. We have two modules in the lab and I believe we can modify these units to work for testing the SSP prototype and revision 1 of the FADC250 that will be ready before the end of FY10. The SD module revisions are effectively only signal pair changes and there are a few other circuit changes that will also need to be included for the final production lot.

December 2009

No significant updates to report. Stay tuned as this module will need to be updated soon.

5. System Diagrams & Test Stand Activities

19 February 2010

See notes in the SSP section, and to repeat, the updated global trigger crate pair mapping has been updated per Ben's request. Sooner than later, this crate pair mapping will be cast in stone and there are ongoing discussions regarding the GTP that may impact the final configuration.

5 February 2010

The Trigger Supervisor crate pair map has been completed and will need to be checked. I believe Ben volunteered to check the diagram. Several other groups have been instructed to use the pair mapping definitions for their front end payload designs, and the pair mapping for the global trigger crate takes into account the signaling required for the SSP-GTP-SD crate scheme.

22 January 2010

The front end crate pair map and global trigger crate map have been updated to reflect the latest decisions for signal interface between the TI and the front end modules. Same note for the global trigger crate, where the TI will interface to the GTP. The Trigger Supervisor crate will also need a signal pair mapping diagram to show how the SD and TD modules will communicate.

8 January 2010

This would be an appropriate place to note the discussion and ideas to test and commission the overall trigger system with simulation data that is loaded directly to the front end FPGA on the flash modules. The method to load these test data to the FPGA through VME has been developed, and there will need to be some software that can assemble and read the simulation data so that the front end channels are loaded properly for a given trigger system test.

Test patterns for a given sub system, would be loaded to the flash boards, and the SSP and GTP would be programmed to trigger if the given test pattern meets the trigger equation criteria. There are numerous possibilities here, and it was proposed to start with the development of software that would read and assemble data from a 'Physics' simulation, and process this data to the front end FPGA through VME. This development effort could start soon, and will certainly be essential once the trigger system is installed in the hall(s). Comments welcome and more discussions will follow.

GTP modules that will reside in the global trigger crate. Other pairs from the SD to the payloads have been changed to accommodate new requirements for additional signals.

Crate Trigger Processor (CTP)

CTP activities are complete.

6. Projects for FY10

19 February 2010

→The original GTP specification was written in April 2008 and discussions have started to at least review the requirement specification and begin an update. We will have to keep this activity moving at the specification stage, because we simply do not have a full time person dedicated solely to this design project. The complexity of the GTP design is an extreme challenge, and we can take advantage of the latest FPGA technology to solve these challenges.

22 January 2010

The GTP specification exists and has not been updated for several months. The activities for the schematic and detailed design issues have not been started and this may slip because the plan was to have a new hire in place by now. Starting the schematic and other activities *could* start soon, but it will impact other project assignments and I do not want to have that happen at this point.

8 January 2010

→Project schedule updates have been reported to the project management team. It has been noted that funding for procurements in the BIA activities are missing, so allocating funding for the purchase of prototypes for SSP, TI/TD etc will have to be extracted from 12GeV funding or a combination with 6GeV operations accounts.

ACTION ITEMS: **Next meeting → Friday 5 MARCH 2010 at 10:00am in F226**