12GeV Trigger meeting notes:

25-Jan-2013: C. Cuevas, W. Gu, B. Raydo, S. Kaneta, A. Somov, N. Nganga, B. Moffit D. Abbott, E. Jastrzembski

18-Jan-2013: C. Cuevas, W. Gu, B. Raydo, S. Kaneta, H. Dong, A. Somov, B. Moffit, N. Nganga

11-Jan-2013: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, E. Jastrzembski, H. Dong, J. Wilson

14-Dec-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga. B. Moffit

7-Dec-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga

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1. *Trigger/Clock/Sync – TI/TD*

25-Jan-2013

→Boards from CEM have not been returned from repair yet.
→Preparing for TS production order can be delayed. There are many test stands that will be setup in the immediate future so the two pre-production boards can be tested extensively.
→TS CODA drivers will need to be tested.
→Dave discusses plans for a significantly large test setup in the Hall D counting room. The activities for this DAQ/Trigger test setup include CODA event builders, testing new ROCs, timing and synchronization. March 2013 time frame is the goal.
→Order yet another TS board for Hall D. Rev2 with changes/correction from Rev1 boards will be ordered. Production version may in fact be Rev2 IF no additional problems are identified.

18-Jan-2013

→New firmware updated for units in the EEL109 global crate test stand.
→No news as typical from CEM, and I would imagine the boards will be here soon.
→CODA drivers for the new TS and latest TI-TD firmware are ready, and the CODA GTP driver has not been developed.
→Hall A folks have three new TI boards and VXS crates will be delivered by the end of next week.

11-Jan-2013

-->Production boards have been delivered to hall groups
→CEM called and gave status on repairs and the boards should be shipped in a few weeks.
→TS and GTP CODA library drivers are in development. This should not delay the global hardware testing though.

14-Dec-2012

→8 TI boards have been returned to CEM for repair.
→Tested production boards have been delivered to the hall groups.
→Need TS front panel

7-Dec-2012

-->20 TD have passed acceptance testing.
→6 TI have known issues and will be repaired at the CM. (Warranty is 1 year)
→2 TI have issues that have not been identified and the problem(s) are not reproducible.
→All other TI have passed acceptance testing. (132)
→Bryan's TS software driver is complete. Ready for full testing and the three crates in the EEL109 lab would be a perfect setup for a full CTP->SSP->GTP-TS->TD->TI test.

1. SUB-SYSTEM PROCESSOR (SSP)

25-Jan-2013
-->2nd week in Feb is the current schedule for production delivery. Partial shipments acceptable but most likely the entire lot will arrive.
→CODA drivers will need development, but firmware for acceptance testing is complete. Final firmware for Hall specific uses is a work in progress.

18-Jan-2013
→1st article board has been accepted and approved by Ben. Production boards will be delivered soon.
→No issues with acceptance testing which is very good news and the acceptance test procedure is close to a final draft.

11-Jan-2013
→1st article board has been delivered and acceptance testing is virtually complete. No issues have been detected. Gigabit serial lanes have been tested and Ben will send the approval for beginning the production run today or early next week.
→Semi-automated acceptance test firmware/software is prepared for the production boards.

14-Dec-2012
→Assembly has started for the 1st article. Board will be at JLAB after the holiday shutdown.
→Front panels designed and sent out for production.

7-Dec-2012
→Bare board delivery will be delayed at least another week due to yield issues, so the 1st article assembly will be delivered in January 2013.
→Existing firmware can be modified to be used with the new SSP. Acceptance testing period for the 1st article is about a week before approval for the production begins.
→PO for the front panel can be awarded anytime.

2. CUSTOMERS

25-Jan-2013
→Discussion about setting up at least 10-12 VXS crates in the Hall D counting house to begin testing of a realistic DAQ system including the event building machines, and other network activities. A significant number of FADC250, SD and TI boards will be needed including TS=>TD and fiber optic links to simulate the trigger distribution path. No plans for using CTP, SSP or GTP for this setup, but it could be a useful setup to verify production CTP, SSP and GTP. For now CTP and GTP production boards will not be delivered for several months.

18-Jan-2013
-->FCAT (Full Crate Acceptance Test) manual has been distributed and reviewed. Automatic checking is not fully implemented yet, but the report file outputs a pdf file.

11-Jan-2013
No report

7-Dec-2012
→Bryan's full crate testing code is in use for the production front-end and triggers modules in F112. The full crate testing is a valuable tool that will verify virtually all interconnections between front end modules and the trigger modules.
→A discussion about using the two TS and two GTP pre-production boards for the initial commissioning of the Hall D Trigger/DAQ system was started and both William and Scott mentioned that there are only a few minor circuit changes that need to be corrected before

starting the production orders for TS and GTP. We know that the Hall B GTP will most likely be the same board used for the front-end crate trigger processing, so it is not entirely clear how many GTP (Trigger Processors) will be manufactured. Again, Hall D can rely on the two pre-production GTP for their immediate commissioning needs.

30-Nov-2012

→A discussion regarding the existing single board computer order was started, and it the focus was regarding the implementation of the PO connection from CPU vendors that are under consideration.

The PCIe protocol appears to be the method that the Concurrent vendor uses, and the plan is to wire at least one full duplex lane from "PP17" on the CTP board. It is not clear how this PCIe lane will be implemented yet, and there may be limitations on the functions/data transfer that can be supported on the CTP.

→Not certain what the status is regarding the full crate testing that is set up in F112. At the last meeting Bryan had made significant progress, and no show stoppers were mentioned. FADC250 boards should start arriving to JLAB soon.

3. *"B" Switch - Signal Distribution Module (SD)*

25-Jan-2013

→Testing is progressing and will need to verify operation with Bryans CODA library.

→Ready to deploy the remote FPGA programming firmware.

18-Jan-2013

-->Serial number and VME remote FPGA programming features have been implemented (90%) in firmware and the instructions for Bryan have been developed.

→OR logic with programmable output 'window' has been developed and tested for use of the FADC250 trig_out bits.

11-Jan-2013

No report

14-Dec-2012

→Serial number storage and VME download firmware are linked and Nick is taking a different approach to implementing these functions. The boards are completely tested, and this firmware will need to be tested thoroughly before distribution. There are software activities that will be coupled to this new firmware as well.

7-Dec-2012

→LUT trig-out logic is tested and implemented in one of the SD boards. The output pulse width from the coincidence of input pulses is programmable.

→Serial Number storage is also firmware that will need to be developed and verified.

→SD Link? Another project at a lower priority.

→VME download function is another firmware activity that can be implemented at a later time.

4. System Diagrams/Fiber Optics

18-Jan-2013

→Patch panels and patch cables have been delivered for the Halls. These will be installed as required by the hall groups.

→Trunk line procurements for Halls B & D will begin soon, and Hall C has already taken delivery of their trunk lines.

11-Jan-2013
→Have received several boxes of patch panels and cables. Will need to check a few out of the batch and deliver them to the hall groups.
→Final lengths of trunk lines will need to be determined soon, and then the order can be placed.

7-Dec-2012
→The PR has been approved for the Hall D and Hall B patch cables and patch panel hardware. Final quotes from selected vendors have not been received, but quantity pricing will work in our favor.

30-Nov-2012
-->Send PR today for approval. This order is for both Halls D and B, and only includes patch cables and patch panel hardware. The trunk line order will be later in the spring when the cable trays are installed.

5. Global Trigger & Trigger Distribution Testing

25-Jan-2013
-→Discussion about the Ethernet connection on the GTP. Cmsg, UDP, DHCP, TCPIP, the normal network definitions need to be defined before beginning the implementation stage. Ethernet interface/hardware has been tested and is functional.
→Global (3 crate) testing is going well and problems are being handled as they show up. Only one FADC250 board in the 'front-end' crate.
→PCIe test boards are ready to send, and the PO boards have already been shipped for fabrication. The switch board will be ordered next week before Scott leaves on travel.

18-Jan-2013
→Scott has been preparing the GTP for production. All ECO will take another week or two.
→Global system test will take a higher priority until Scott leaves for Trigger School.
→PCIe test boards have been designed and the switch card will be ordered soon.

11-Jan-2013
→Global crate testing is progressing but will need Bryans help soon to complete the measurements.

14-Dec-2012
→PCIe test boards in the design queue. The switch test board will need an oscillator, but the other boards will be simple passive boards to pass the appropriate serial lanes.

7-Dec-2012
→Scott presents an idea to allow for the use of all four serial lanes from the FADC250 boards to be tested with the CTP and GTP. Recall that the CTP interfaces only TxRx3-4 from the payload slots. The Concurrent CPU uses TxRx11-2 for PCIe lanes, so Scott's idea is to build a few passive circuit boards that connect the lanes as needed for testing.
→Getting closer to measuring the complete round trip latency with the three crate configuration in EEL109, and several other important measurements need to be verified and recorded with this test. If there are no significant hardware problems identified with the pre-production TS and GTP boards, then proceeding to the production activities can begin soon.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

25-Jan-2013

→Acceptance testing procedure and firmware is in place for testing the production boards.
→Phone meeting with PCB manufacturer was very useful and the CTP layer stack will undergo a few modifications. Good news is that the BOM and solder paste stencils have been ordered.
→Final front panel design work should be completed soon and tested on the 1st article board.
→It is time to create a requirement document for the Hall D Tagger application. Rather than the CTP performing a total sum, the CTP will collect "hit" information from the Microscope and Hodoscope detectors in the Tagger sub-system. Many details to list and a document must be generated.

18-Jan-2013

→Site visit to MTEQ on 9-Jan-2013 went well and was fully approved by the JLAB QA/QC division.
→Final BOM and fabrication files are at the vendor! The production contract shows a 12 week delivery for 1st article and then 12 weeks after approval of the 1st article for production deliveries.
→Manual for the automatic testing and I^2C firmware download is in progress.
→Front panel and heat sink machine work needs to be started.

11-Jan-2013

→Fabrication files are ready for final check and will be sent to MTEQ next Tuesday.
→Acceptance test program is ready. 12week delivery of 1st article then 12weeks for production run after we approve the 1st article.

7-Dec-2012

→Routing strategies have produced a fully routed board and final checking is in progress. There are a few items that need to be changed but overall Jeff and Hai are on track to deliver Gerber and NC drill files to MTEQ after the holiday shutdown.
→The final BOM has been transmitted to MTEQ and the alignment keys have been purchased. These alignment parts will be assembled at JLAB. Heat sinks have been ordered and will be machined and sent to MTEQ for the final assembly. The front panel design and order will need to be completed soon also, and delivery of the 1st article board is 12wks from receipt of the fabrication files.

***ACTION ITEMS*: Next meeting - Friday 3 February 2013 @10AM in F227**