12GeV Trigger meeting notes:

7-Feb-2014: C. Cuevas, W. Gu, B. Raydo, B. Moffit, E. Jastrzembski, H. Dong, A. Somov, J. Wilson

24-Jan-2014: C. Cuevas, W. Gu, B. Raydo, B. Moffit, E. Jastrzembski, H. Dong, A. Somov

10-Jan-2014: C. Cuevas, W. Gu, B. Raydo, A. Somov, B. Moffit, E. Jastrzembski, H. Dong, J. Wilson

13-Dec-2013: C. Cuevas, W. Gu, B. Raydo, A. Somov, B. Moffit, E. Jastrzembski, H. Dong

6-Dec-2013: Canceled

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1. *Trigger/Clock/Sync – TI/TD*

7-Feb-2014

> TI Masters working well for FCAL and BCAL south.
> Move trigger crates to the hall as soon as trigger racks have power.
> TD, TS and SD crate will be installed, and the boards will be provided by Alex
> Will need to configure a few more TI to work as TI_Masters.
> TD <-> TI Link Identification feature tested and complete? Work in progress,

24-Jan-2014

- TI-Master configuration is working on FCAL. This configuration will remain permanently and the global link will occupy one port on the TI's. Other detector crates may be organized with the TI-Master mode as well. This will require additional fiber transceivers and fiber patch cords.
- TD <-> TI ID feature tested with CODA3? Will be ready for future CODA 3.0.release.

10-Jan-2014

FCAL TI-Master configuration is progressing and as soon as the trigger fiber is installed the CTP boards and TI can be hooked to the global distribution crate. 14-Feb-2014 is my predicted installation date.

13-Dec-2013

Discussion on implementing the FCAL cosmic test. The production SSP and CTP should be tested in F117 before moving these boards to the hall.
→TS -→TD crate is ready to move to the hall. Firmware for TD <-> TI ID information is ready. Not implemented in CODA3.

1. *SUB-SYSTEM PROCESSOR (SSP)*

7-Feb-2013

- SSP end is ready for testing, but CTP side is work in progress.
- CODA library for SSP will be tested and verified by Bryan before release.
- Started loan paperwork for additional SSP that will be loaned to Saclay (uMegas)

24-Jan-2014

- CTP → SSP ID link firmware has been updated. Library development in the queue.
- Hall A application is work in progress, and a meeting is planned.
- Send at least 4 SSP to Saclay.

10-Jan-2014

- Ben and Hai have settled on the method to transfer the information that will identify the CTP through the SSP link.
- Some changes will be needed to the driver libraries for the SSP. (CTP too?)

Testing and library verification can be completed in the EEL109 test stand.

- Hall A application for the SSP! Need to get details from Alexandre and J. Musson.

13-Dec-2013

-->Define registers for ID information between CTP → SSP links. Presently this ID info is not implemented. Lower priority, but from my understanding of the discussion this ID info should not be too difficult to define, implement and test.

2. CUSTOMERS

7-Feb-2013

- Mode 6 is RELEASED! Hai and Ed have made it bullet proof!
- Firmware Priorities:

CTPV2 testing - Complete (30 of 33 boards passed)
Mode 6 repair - Complete
BCAL cosmics
- Changes to the CTP for 'hit bits'
- These bits are already defined for the SSP
- BCAL/FCAL (FADC250 changes to trigger output data)

Tagger Hit bit application
TOF application
Pair Spectrometer
CTPV2->SSP ID

24-Jan-2014

- Hai said (with witnesses) Mode6 will be ready by end of January 2014.
- CTPV2 contract is in the process of termination. 30 of 33 boards were completed.

Hall D has all the boards they need for commissioning.

10-Jan-2014

→Mode 6 even closer to release! Bug fixes are in progress.

13-Dec-2013

-->Modifications are still pending for the 'Mode 6', bugs identified and further testing will be required before final version released. Firmware modifications should not require any library (driver) changes.
→I believe the PCAL folks (Hall B) could still be the 1st detector group to use this Mode 6 with a full crate of FADC250.

3. "B" Switch - Signal Distribution Module (SD)

7-Feb-2014

- Not a high priority but Ed has compiled Nick's project, so testing will progress as time permits.

24-Jan-2014

- Still a few bug issues with the A5 release.

Maybe William and Ed can investigate??

4. System Diagrams/Fiber Optics

7-Feb-2014

- 3 more spools delivered for FCAL run. Tagger spool is on the way. Install week of 10-Feb.
- Order short patch cords. Plenty of 2m cables for crates to patch panel connections.

10-Jan-2014

- 5 of 11 trunk lines are installed and tested.
- PR signed for 4 more trunk lines for the FCAL and Tagger.

8-Nov-2013

→It has finally happened, 5 of 11 fiber trunk cables have been ordered!! Will need to coordinate installation with Tom Carstens (Hall D) and will also need to measure lengths for the FCAL and Tagger tunnel areas. Fortunately the cable is a stock item, and it will not take long to install and test the short lengths.

5. Global Trigger & Trigger Distribution Testing

7-Feb-2014

- Version 1.0 has been released for the GTP firmware. Document is updated and includes all the latest register definitions as well as a new section that describes the embedded Linux addition.
- CODA3 Library driver development will begin.

24-Jan-2014

- Linux OS is stable and ported to the GTP NiosII processor. Chris H. has completed the sections relevant to the embedded code and has updated the GTP manual.
- Ben has signed off on the release and is using the embedded Linux OS on the production GTP boards.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

7-Feb-2014

- Contract has been cancelled and new PR issued for replacement of 3 boards
- Discussion with procurement and 12GeV PM to find funds for an additional 2.
- See 'Customer' section for activity priorities for CTPV2 firmware.

24-Jan-2014

- 3 of 33 still have a few issues. Hall D has 30 boards!
- Two of the boards will need additional rework to swap parts to the correct location. MTEQ is working with their sub-contractor to get these two boards finished.
- One board has significant issues and will take sequential rework to identify which BGA is the problem.

13-Dec-2013

- 8 boards delivered to MTEQ on 9-Dec-2013 and we already have a rework plan from them and several of the boards have been sent to a sub-contractor for 3D X-ray. We estimated that these boards should be back to JLAB by 17-Jan-2014.

8-Nov-2013

→25 of the 33 production boards have passed acceptance testing and are loaded with the latest firmware. Hai has completed testing of the remote firmware download feature, and the working boards have been delivered to Hall D. (Alex)

→Preparations to send the boards that need rework back to MTEQ are underway and by 9-Dec-2013 we will ship these CTPV2 boards using a new RMA. Round 2!

ACTION ITEMS: **Next meeting -Friday 14-Feb 2014@10:30AM in L210A**