12GeV Trigger meeting notes:

24-May-2013: C. Cuevas, B. Raydo, A. Somov, J. Gu,N. Nganga

17-May-2013: C. Cuevas, B. Raydo, A. Somov, J. Gu, S. Kaneta, E. Jastrzembski, N. Nganga

10-May-2013: No meeting

3-May-2013: C. Cuevas, B. Raydo, A. Somov, J. Gu, N. Nganga, H. Dong, J. Wilson, H. Dong

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1. Trigger/Clock/Sync – TI/TD

24-May-2013
→PR has not been sent but will be submitted next week for remaining TS production modules.
→New front panels for master TI boards will be ordered.
→TS meeting within the DAQ group and there will be firmware changes forthcoming.
→Review the Hall D layout and plan for grouping readout crates in order to come up with a count of required TI-Master boards.

17-May-2013
-->Final count for TS production modules for all halls is 7-10 boards. William is ready to submit the PR and will need signatures soon.
→10 TI boards have been sent (and received) to be converted to master TI mode. William is in the process of acceptance testing.
→The 12 crate CODA test setup in Hall D has produced firmware modification requests by Dave Abbott. These changes affect the trigger distribution hardware (TS, TD, SD, TI)

3-May-2013
→Next week begin the procurement and document review for more production TS boards. It is not clear if Hall A will use/need a TS but before the order is placed ALL the halls should consider the quantity for the production order.
→The production TS board has the addition of line receivers for the LVPECL signals from the DensiShield cables. These receivers prevent the increase of current on the drivers when the TS is powered off. At some point soon, the production TS will be moved to the Hall D CH for testing, so a pre-production TS will be used the Global Test Stand. Be aware that the pre-production TS in the off condition will cause extra current for the GTP DensiShield cable drivers.

1. *SUB-SYSTEM PROCESSOR (SSP)*

24-May-2013
→SSP boards can be delivered to the hall groups, but further testing and firmware changes will be on hold for some time.
→SSP firmware has been modified so that the SSP can act a CTP generator so that the SSP to GTP data streams can be realistically delayed to simulate different front end crate data delays.
→Investigate transceiver laser class hazards and IF mitigation is needed.

17-May-2013
→Two production boards have been delivered: 1 for Hall D, and 1 to Hall B(CEA Saclay)
→Use the SSP for a power supply test today or Monday.

3-May-2013
→All SSP boards have been acceptance tested. No significant issues noted.

→Fiber transceiver parts are installed for each of the 8 ports

19-April-2013
→Acceptance test code is close to completion.
→Final draft of the JLAB VXS L1 Trigger Protocol document has been created by Ben and includes many details of important items that will be required for diagnostics during Physics production runs. Lots of implementation and other development work will be needed.
→Start thinking about using one SSP to fan-out fibers to multiple SSPs in the global crate. The best opportunity to try multiple SSP will be in the Hall D CH.

2. CUSTOMERS

24-May-2013
→FCAT developments for every full crate setup. i.e. F1TDC, FADC125, Discriminator.
→SBC that will be shipped to CEA Saclay is ready for loading the bootRom.

17-May-2013
→GTS now has histogramming features for plotting the results from tests in the EEL109 test station.
→One crate in F112 appears to have a Sysreset line stuck. Bryan mentioned that it may be a controller, but it may be an active chip on the backplane. Fernando has replaced the fan tray and power supply but the problem remains. Further discussion reveals that this issue should be investigated and listed so that other folks know about the problem.

3-May-2013
→It would be interesting to see initial results from the 12 crate DAq testing in the Hall D CH. Will ask Dave A about a presentation at an upcoming trigger meeting.
→NSU FADC250 boards are in EEL109.
→Begin to plan for the FADC250 test station activities.

3. "B" Switch - Signal Distribution Module (SD)

24-May-2013
→Test GTS with SD PLL enabled.

17-May-2013
→PLL parameters will need to be adjusted for the F1TDC crates (31.25MHz) and the FADC125 (125MHz).
→Good discussion on PLL settings and present run/test conditions with the existing test stands. I believe all settings for test stands are set for the default.(NO PLL).

3-May-2013
→The SD production boards are enjoying an excellent transition to the installation phase and no issues have been discovered. There are a few firmware development projects to continue, but these developments are not critical.

4. System Diagrams/Fiber Optics

15-Mar-2013
→No action until cable trays are installed in the halls.
8-Mar-2013
→No report.
8-Feb-2013

→Patch panels and patch cables are being checked in now, and will be distributed to the hall groups
→START procurement for trunk cables in D and B by May??

5. Global Trigger & Trigger Distribution Testing

24-May-2013
GTP boards have been sent to Advanced Assembly in CO. Expect full assemblies by July.

17-May-2013
→Production GTP PCBs have a bit of delay and Advanced is ready for the bare boards. Two production boards will be delivered by July.

3-May-2013
→Scott had a presentation prepared for last week, but he meeting was canceled. His slides have been posted to the wiki. The overall trigger latency has been measured at 2.7us and the effort to reduce this time is significant and appreciated. There are several transmission latency paths that need to be measured and documented, (see slides) but the large latency paths are well known and cannot be reduced. (fiber cable delays)
→Trigger Processor (CLAS12) proposal has been circulated and the Hall B folks have generally accepted Scotts proposal. Review of requirements and cost estimates for the proposed FPGA solution should be performed again.
→Production GTP bare boards will arrive next week from ACE and the assembly will begin soon after that. The assembly was awarded to Advanced Assembly so this project is on schedule.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

24-May-2013
→Phone conference yesterday and the CTP is ready for production!
→Not ready for testing in the GTS but refinements to the automatic test code for production acceptance will be the focus.
→Production delivery schedule will be updated by the contract manufacturing.

17-May-2013
→Approval for production will be sent next week.
→Acceptance testing is complete except for one of the configuration devices.
Hai is at MTEQ today so they can replace the part and he will confirm that it is not the FPGA.

3-May-2013
-->Acceptance testing is going well.
→Transmit final BOM to MTEQ
→Front panel prototype adjusted, and updated files will be sent to machining shop.
→Send approval to MTEQ soon.

***ACTION ITEMS*: Next meeting - Friday 31 May 2013 @10AM in TBD**