12GeV Trigger meeting notes:

19-October-2012: Meeting cancelled

12-October-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, Beni Z. H. Dong, N. Nganga, B. Moffit

5-Oct-2012: Cancelled (Hall D Collaboration Meeting)

28-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, B. Moffit

21-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, B. Moffit

14-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, J. Wilson, B. Moffit

7-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, E. Jastrzembski

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0. Trigger/Clock/Sync – TI/TD

12 Oct-2012

→Deliveries of next batch of production boards unknown. Will receive schedule today.
→Repaired board has passed acceptance testing.
→William distributed a message regarding trigger latency measurements and there have been several discussions:

> The minimum TS to TI latency using the 62.5MHz trigger 'link' is rather long and is approximately 570ns. If the internal logic operates on a 125MHz clock this latency period can be reduced. Fiber distribution will add to this latency delay, and in the end the minimum requirement is 3.5us to be sure that timing hits are not lost for the F1TDC board.

→Changes to the TI-TD firmware is close to complete. Testing activities to begin soon after the firmware revision is ready.

28-Sept-2012

→CEM repaired the bad board and returned it to JLAB. William has tested the board and it passes the acceptance testing.
→The TI firmware has been changed so the version 1 boards will need to be updated with the latest firmware. The version 2 boards have the latest firmware. Bryan has the new CODA library for the version 2 boards.
→TS development work is on hold, and the front panels will be here next week. Two TS boards are fully populated and functional. Prepare for global test stand testing soon.

21-Sept-2012

→Acceptance approval memo has been delivered to the CEM and procurement.
→Rework/repair of the bad board should be complete next week. CEM sales rep will return the board.
→V1290 TDC fan-out board supports eight boards. More are needed for both Hall B and Hall D.
→Ask the Hall C and A groups about their requirements for the V1290 TDCs.
→Final delivery for the TI-D procurement is listed for Feb-2013
→Production firmware is ongoing. New CODA library will need to be update.

14-Sept-2012
→Production acceptance approval is due next Monday 17-Sept. The one bad board has been given to the sales rep, and the part will be x-rayed.
→14 of 15 boards are undergoing tests, no issues recorded.
→Trigger Supervisor testing: The TS Fpga uses GTX transceivers which will need adjustment in firmware.
→V1290 TDC fan-out board is complete. This fan-out board supports 8 TDCs.

7-Sept-2012
→Testing is progressing nicely. 1 of 15 boards has a power supply issue with the -5v.
→TS work is not the highest priority, and a CODA library exists
→Multiple crates in the DAQ lab to test the configuration and fiber drivers between TI and TD boards including an SD module.
→After acceptance test report is completed, CEM has 20 weeks to deliver the balance.

1. *SUB-SYSTEM PROCESSOR (SSP)*

12-Oct-2012
→An internal review of the fabrication data is imminent. Ben will continue to verify the new layout and set up a meeting time.
→Front panel and other peripheral work continues.

5-Oct-2012
→90% routed and the manufacturing files will be reviewed by several folks.
→Zentech has ordered the parts
→Still on schedule for sending files. 1st article due 8weeks after files and parts received.
→Acceptance testing code etc needs to be completed. Re-use of many routines from original SSP work can be used.

28-Sept-2012
-->Letter of increase needs to be approved for additional cost of extra layers. The cost can be split to the different groups.
→One additional board will need to be added to the contract for Hall A
→Manufacturing files are progressing nicely and a final review will be scheduled soon by Ben.

21-Sept-2012
→Letter of increase to support extra layer requirement for production SSP boards and PRs for front panels will need to be approved. Use same POAs for front panel and miscellaneous hardware requisitions.

14-Sept-2012
→Parts will be received at Zentech on 17-October. Gerber files and other manufacturing data are due soon.

7-Sept-2012
→Zentech is proceeding with the BOM purchase. Some long lead times, so final route files not due for about a month.

2. *CUSTOMERS*

12-Oct-2012
→Full crate testing activities are imminent and FADC250 production boards will be here soon. Will need to re-use a CPU and CTP to complete the crate test.
→CPU production order is in the process of receiving evaluation models.

28-Sept-2012
→Global sketch to show collaborators where/how to use signals to trigger pulsers, LED etc.
→Full crate verification testing will begin soon. (mid October?)

21-Sept-2012
→New topic for the Hall D BCAL trigger scheme. Presently just an idea, but as always, the development of new firmware will have to be considered.
→Initial beam running will be low luminosity, so the trigger will be derived from the tagger hodoscope and microscope.
→Hall D collaboration on 4-6, October and Hall B Collaboration the following week would be good opportunities to discuss other interesting trigger topics.

3. "B" Switch - Signal Distribution Module (SD)

12-Oct-2012
→112/115 have been tested and passed.
→Distributed 58/60 to Hall D
→3 have been sent to CEM for rework/repair

28-Sept-2012
→70/115 have been tested and passed. No issues to report.
→

21-Sept-2012
→CTP#4 was located in EEL109 and is loaded with the SD-test firmware.
→113 boards have been received with two remaining at the factory.
→25 of 115 have passed acceptance testing
→Full steam ahead on testing in the full crate and so far no assembly issues have been discovered.

14-Sept-2012
-->Need a CTP. Need to check where the #3 board is located so Nick can continue testing.
→Received 30 production boards.
→25 of 115 boards have passed acceptance testing.

7-Sept-2012
-->49 production boards have been delivered
→Remaining 55 boards will be here soon.
→SD test station is ready to go.

4. System Diagrams/Fiber Optics

12-Oct-2012
→No update. A recent walk through of Hall D shows virtually zero cable trays or equipment racks. Trunk cable order will be dependent on the accurate lengths from the trigger racks to the various detector readout racks.

28-Sept-2012
-->New transceivers have been received and there are a few parts to order.

21-Sept-2012
→FO patch panels and other hardware have been received for the Hall C trigger fiber installation.
-->Fiber trunk cable for the Hall C order can be tested with new Fluke meter and also in the EEL109 lab using trigger modules in the Global Test setup.

14-Sept-2012
-->Review FO diagram with Brad. Prepare for installation.

5. Global Trigger & Trigger Distribution Testing

12-Oct-2012
→SSP->GTP testing is going well. The next step is to integrate the GTP output (all 32 bits) to the TS-SD-TD crate. Run at full trigger rate, use adjustable delay (processing time) in GTP and then ultimately connect to the front end crate to measure FULL system latency.

28-Sept-2012
-->Another VXS crate has been installed in EEL109. This will be used in the Global Trigger testing.
→Still need to locate a CPU and TI.
→Ultimate goal is to measure and record the final latency from the GTP → TS → TD →TI

21-Sept-2012
→TI communications established through I^2C to GTP
→Register map definitions created by Scott and drivers developed by Bryan
→Third VXS crate moved to EEL109 lab. This unit will be configured as the Global Crate with SSP->GTP. Will need SD and ROC plus TI. The Densi-Shield cable will reach the Trigger Distribution crate and interface with the TS on the rear transition panel without issue.

24-Aug-2012
→Time to get the hardware mounted in the rack:
--1st crate – Global – SSP (FADC250), GTP, SD, TI
--2nd TS, SD, TD
--Densi-shield cables. Use two cables for now (15 trigger bits + clock)

17-Aug-2012
→Scott continues to test the GTP using FADC250 boards as the data generators. VXS Gigabit serial links are running @5Gb/s with a few errors, but long term data is needed to increase our confidence level to operate at the higher bit rates.
→No VME backplane readout is exercised during the serial tests, and 2eSST readout should be exercised during the 5Gb/s serial data transmission testing to replicate a real system test. What should the duration of the testing?

10-Aug-2012
→16 FADC250s used as data generators to GTP @5Gb/s with some errors, but over a 48 hour period. Good news. No equalization parameter adjustments yet, but this could be tested and documented.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)

3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

12-Oct-2012
→The production order for Hall D CTP was cancelled by the vendor. The new RFQ will be posted soon and there are no changes to the specification or BOM.
➔ Board routing is progressing and with the new bid process we have gained a few weeks of routing and verification time.
➔ Hai is very close to completion with the CTP automated acceptance test procedure.

28-Sept-2012
-->A week away from full time routing on the CTP. F1TDC projects will take some time, but will be finished soon.
→CTP kick off meeting is 2-Oct-2012 with the Zentech folks.
→BOM will be discussed and parts need to be ordered now so any long lead items are available by the time the boards are fabricated.
→Production acceptance test code is at 65%.
→Work by Scott was shown regarding effort at pin swapping to improve routing.

21-Sept-2012
→Jeff is very busy, and the schematic changes and net swapping list is progressing.
→Final BOM is important and needs to be ready to send as soon as the award is final (2wk of Oct?)
→16 layer circuit board is the goal, or additional funding requests will need to be generated.
→VHDL firmware for the acceptance testing of the production CTP is at 60%. This will take a lower priority because the production FADC250 test procedure program needs modification.

14-Sept-2012
→Evaluate low bid paperwork. Need a decision by Monday 17-Sept-2012
→Continuing on the layout, a few schematics need to be corrected and then the full routing plan will ensue. BOM needs to be updated.
→CTP acceptance test development is in progress.

7-Sept-2012
→CTP automated test is 50% complete
→Production TI will be ready for Hai in two weeks.
→Jeff is on vacation, routing the CTP is on hold.
→Bids are due 7-Sept. Lowest price wins.

GTP and Global Crate Developments

12-Oct-2012
→ECO list prepared for GTP final version
→Work continues with the Global crate test setup.
→2nd GTP prototype has been assembled and tested.

28-Sept-2012
Notes on Global setup and Root development.
Ethernet stack code from Hai appears to work fine and compiles with Altera device.

21-Sept-2012
→SSP firmware is in rework to be used for the global (GTP) testing.
→Move a (Hall B) VXS crate to EEL-109 for dedicated testing of the global hardware.
→Beg, borrow, and steal CPU, SD, and TI, to keep in EEL109 until hardware testing is complete for the global hardware.

14-Sept-2012
-->Turnkey order for single GTP has been approved.

7-Sept-2012
See Scotts presentation

***ACTION ITEMS*: Next meeting - Friday 19 October @10AM in F226**