12GeV Trigger meeting notes:

29 July 2011: C. Cuevas, J. Gu, E. Jastrzembski, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo

15 July 2011: C. Cuevas, J. Gu, E. Jastrzembski, A. Somov, N.Nganga, Bryan Moffit, J. Wilson

8 July 2011: C. Cuevas, J. Gu, B. Raydo, E. Jastrzembski, H. Dong, A. Somov, N.Nganga, Bryan Moffit, C. Dickover, J. Wilson, S. Kaneta

1 July 2011: C. Cuevas, J. Gu, B. Raydo, E. Jastrzembski, D. Abbott, H. Dong, S Somov, N.Nganga, Bryan Moffit ,

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0. Trigger/Clock/Sync – TI/TD

29 July 2011

Acceptance testing is going well with six boards working well, and 4 boards have issues with power supplies. (LGA). These boards will be returned to the assembly vendor for rework/repair. One TI-D has been tested with all eight optical transceivers operating at the same time and firmware for the Master TI is ready

15 July 2011

→TS design and layout is virtually complete! William is ahead of schedule for the prototype TS revision. Layout has been reviewed and we will plan to have a separate meeting to discuss critical details of several circuit functions before sending manufacturing data for fabrication.
→TI-D pre-production modules have been received and are in the process of acceptance testing.

8 July 2011

→The 10 pre-production TI-TD boards are at the assembly vendor. These boards should be received during the week of 11-July. William has an acceptance test plan in place for these boards.
→William has distributed a link to the latest Trigger Supervisor (TS) board layout files. I think it would be a good time to review the TS requirements and verify the TS functions of the existing TI design before moving on to the initial TS board fabrication step.
→Bryan reports that the firmware corrections have been implemented in the TI boards so that the ROC ACKnowledge works correctly and both crate TI are synchronized.

1 July 2011

Document outlining the DAq run modes has been created by D. Abbott and discussed at last meeting.

We will need a detailed document defining the TID→SD→TS signal management for the ROC ACKnowledgement mode. The TID must manage up to eight fiber optic serial link information streams from front end crates. Each link carries important information that needs to be transmitted to the Trigger Supervisor. The Trigger Supervisor has a slightly different P0 map as compared to the TI, and the signal path from the SD slot has enough signal pairs to manage the TID information. More block diagrams, and detailed circuit function descriptions will only help.

It is not too early to begin a rough draft of startup procedures, flow charts, etc for the two crate test station. At some point the two crate test station should be close to a 'turnkey' operation so that we can verify a full crate of new front-end DAq and trigger modules.

Ten Rev4 TI boards have been sent to the assembly vendor. These boards have a ten day delivery, and will be tested thoroughly before distribution to detector groups.

2. *SUB-SYSTEM PROCESSOR (SSP)*

29 July 2011
Ready to go for full crate testing!

8 July 2011
→The SSP prototype has been put to good use in the two crate test station, and the design has been ahead of schedule for quite some time. The schedule to fabricate and assemble the production quantities has been pushed to the middle of FY12. Only very minor changes to the prototype design are required before sending the SSP for turn-key production.
→I am certain that the firmware (applications) for the SSP will continue to evolve and there are other groups that have already considered the use of the SSP for their readout purposes. (CLAS12 – SVT and uMegas detectors)

1 July 2011
No report, but good discussion and presentation by Ben on event display work so far. Bryan and Ben have been working on the plotting routines for the two crate test stand data. Methods to reduce the amount of data stored to disk are a work in progress.

3. CUSTOMERS

29 July 2011
Meet on Monday 1 August to establish priorities to test problematic boards that did not pass acceptance testing. Deliver two boards to Injector group. Latest firmware can be downloaded in situ.

15 July 2011
→22 of 33 FADC250-V2 boards pass the initial acceptance testing phase! We will have at least one full crate of boards by the week of 25-July-2011.
→The order for 4 additional boards has been received. These boards are reserved for the Injector and the Medical Imaging groups and have passed the acceptance tests. These boards can be delivered to these groups soon.

8-July-2011
16 FADC250-V2 boards will be here week of 11-July-2011. Plenty of preparation work before testing can begin. We will make it a goal to have 16 boards ready for at least one crate by the week of 25-July! So far the acceptance testing is going smooth!

1 July 2011
A full size VXS crate is in the EEL109 lab on the bench for the acceptance testing of the pre-production boards. We expect the box of boards to arrive the week of 4-July-2011 and then many activities will need to be completed before we have a full set of FADC250-V2 in the test stand crates.

4. "B" Switch - Signal Distribution Module (SD)

29 July 2011
Six boards are at the assembly company with a two week delivery schedule. Expect delivery of the assemblies by week of 15-August.
Nick is finalizing the acceptance test code for the SD boards and will continue to update the specification document for the SD module to include the latest revisions to the control registers etc.

15 July 2011
Delivery of boards next week then on to assembly
Acceptance test firmware in development.
New I^2C function for the latest SiLab PLL
A few PRs for some missing parts need to be ordered.
Need front panel material (blank panels and ejector-injectors)

8-July-2011
-->Nick has ordered the circuit board fabrication and the award for 6 boards has been placed with Colonial Circuits. The assembly job will be completed by Advanced Circuits and a delivery schedule is forthcoming.
→Now is a good time to update and complete the SD documentation and the test firmware for the initial acceptance testing. Minor changes to final firmware will need to be documented and propagated to Bryan and William for the control interface.

1 July 2011
→Fabrication files and schematics have been reviewed and Nick has prepared the purchase requisition for six pre-production units. Cost estimates have been received, and the parts kit is ready for shipment to the assembly company as soon as the order is placed. 12GeV funding has been defined, so the order is imminent.
→Documentation will need to be updated to reflect the latest ECO including new firmware descriptions for the SiLab PLL control.
→Test firmware and test procedure will need to be completed soon, so the SD-Rev2 boards can be tested as soon as received from the assembly company.

5. System Diagrams/Fiber Optics

29 July 2011
No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

15-July-2011
DRAFT version of the specification is almost ready for review.
The diagrams for Hall D and Hall B have been checked and will be included in the specification document to show the installation details of the parallel fiber optics required for the Halls.

8-July 2011
No report, but 15-July deadline is looming(Chris).

1 July 2011
→System level fiber optic distribution drawings are complete for both Hall D and Hall B. Initial estimates for cost of the patch panels, patch cables, and trunk cables have been received, but procurement will need several vendors to bid on this work.
→Fiber optic specifications are a work in progress and will be in draft form by 15-July-2011. (Chris)

6. Two Crate DAq test configuration

29 July 2011

- ➔ At least 20 FADC250-V2 boards are populated into two VXS crates in the EEL109 lab. There are a few critical firmware items that remain to be completed before reaching the goal of 200 KHz trigger rate.
  - Firmware for 2eSST working with Token passing
  - CTP must be programmed to receive Gigabit serial data from each of the 16 payload slots.
  - Did I forget anything?!
- ➔ Running in "Playback" Mode
  - Firmware and software exists to configure the FADC250 boards with data that will be cycled with the Trig_2 signal. The "Playback" Mode will allow deterministic testing of the energy summing, and Bit_Error_Rate (BER) testing. The "Playback" Mode also allows testing of every channel without cabling input signals.
- ➔ The following is a copy of the test goal list created several months ago:
  - **Goals of the integration testing:**
  - **-Verify clock distribution through TID->SD and measure jitter to front end boards**
  - **-Verify trigger rate and readout rate for a variety of occupancy levels.**
  - **-Verity token passing scheme**
  - **-Verify CTP operation with sixteen FADC250 @2.5Gbps**
  - **-Test playback mode feature on two crates and verify operation with SSP.**
  - **-Measure and record overall trigger latency. (Could include SSP)**
  - **-Verify full 2eSST readout from payload modules**
  - **-Verify TI-D features and use one TI-D in TS 'mode'**
  - **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**

15-July-2011

Coordinate 16 boards with Fernando and Fabian. Analog test signal for every input, data is stored and needs analysis. When can we move 16 boards to the test station?

Playback mode discussion. This would be a perfect method to run deterministic data from each ADC channel and compare readout data to "stimulus" data. Will also allow for BER testing of full system. Final sum information at SSP can be verified as well.
Firmware supports the playback mode, and there are software functions that support the playback mode. Playback signal data can be loaded to front end FPGA and playback is initiated with the Trig_2 signal.

8-July-2011

→Bryan reports that he was able to operate the two crates in ROC-ACK mode @25KHz with the two FADC250 boards each converting two channels.

- 2eSST readout is used for readout
- Two different Linux ROCs appear to be working fine using the polling method with the TI
- Block size is 1 trigger(event)
- Synchronization between two crates appears to be resolved
- More channels will be added to each FADC250 module

→Bryan presents several plots that show the ROC readout times and other useful readout diagnostic displays.
→Time to increase the block size and test the full pipeline trigger mode to answer the questions of how high can the trigger rate go, and how long at the high rates will the system remain stable.

1 July 2011

→Progress continues on the diagnostics tools/plotting routines to display important information while running the two crate test.

→Not sure where we stand on resolving the synchronization issue between crates, and the focus to run the two FADC250 boards for a long duration at high trigger rates has been compromised because of other technical activities as follows:

-Busy 'level' not programmable? (Ability to set the point where BUSY is asserted)
-Troubleshooting DAC offset issue
-Work on subtracting pedestal values has been started.

3 June 2011

→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

→ Ben presented a few oscilloscope photos and Chipscope plot from the SSP. The SSP plot clearly shows the two signals that were injected into each FADC250. One signal was delayed by 15ns and the SSP 'history' plot shows these signals clearly. There are several small issues to clean up with how the SSP handles the data bytes from the CTP, but it appears that the hardware is working and is ready for further testing.

→ There was a discussion on how the DAq was configured, i.e.) Handshaking, and what run mode was configured? It appears that the system was operated in non event 'blocking' mode. The trigger count matches from each module in a crate, but the trigger count information crate to crate do not match. What is the difference? Why?

→ No Token passing scheme was used during the single FADC250/crate test but 2eSST used for readout.

What is the BUSY 'high water' threshold setting?

→ Issues:

Synchronization MUST have this working flawlessly for high rate testing.

Data integrity, Need some Data plots to show trigger rate Vs readout data size.

Comparison tables for 'scalers' for a each module within a crate and comparisons between crates: Trigger count from each board, Busy counter? Other?

22 April 2011

The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→Goals of the integration testing:
-Verify clock distribution through TID->SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point) See older note dates for the list.

6. Crate Trigger Processor (CTP)

29 July 2011
CTP work will be 2nd priority after the FADC250V2 troubleshooting period. Hai has started testing a CTP with sixteen loop back connectors, and results are promising. Hai will need 16 FADC250V2 to verify his latest CTP firmware, and then the CTP can be installed in the two crate test station. At some point the 'broken' CTP needs to be repaired.

15-July 2011
No report.

8-July-2011
→CTP3 appears to have a problem with loopback test. CTP4 appears to be working with loopback at 2.5Gb/s with six payload ports. Possible issue with voltage regulators on CTP3, could be the culprit. Hai will be on vacation during week of 11-July and has started the development of automatic functional test firmware for the CTP.
→Firmware additions will be needed to implement 16 Gigabit Transceivers for each CTP. This is the first time we have had more than six FADC250 at one time!

1 July 2011
→So far, CTP1 and CTP2 are used in the two crate test station. These CTP are the original two units with Virtex 5 'LX110 devices. CTP3 and CTP4 have Virtex 5 'FX70T devices and should be able to run at 5Gb/s. Hai has started testing with CTP 3 and CTP 4 to verify functional operation before testing with the FADC250.
→Need to review ECO list, and other revisions soon, and establish a schedule for the implementation of the CTP changes.

7. GTP and Global Crate Developments

29 July 2011
The partial (power) board will be shipped the week of 1-Aug. It is a very prudent step to verify and fully test the power board and then proceed with testing of the board that was fully populated.

Acceptance firmware: Development work is a work in progress.
Document is in progress. Updates to specifications should reflect latest hardware revisions.
Full crate could be used to test the Xilinx Aurora protocol with the Altera Transceivers.

15 July 2011
→The 1st board is at the assembly company and will be partially populated with the power section components only. 2nd board has been received, inspected and shipped to the assembler. After verification of power section, the 2nd board will be fully populated.
→Acceptance test firmware is progressing and will need to be comprehensive for all the GTP sections.
→Crate level testing can be accomplished by using the Gigabit transceivers on multiple FADC250.
→Acceptance test plan and procedure document is in progress

8-July-2011
→Scott received the 1st board and a solder sample board. These first revisions are RED so it should be good luck! Initial board and components have been sent to the assembly company

and will be partially assembled with only the power regulators for test verification. After power section has been tested, a single board will be fully populated.
→Firmware working with the BeMicro kit for Ethernet access features. There was a discussion on testing a GTP using 16 of the FADC250 boards, which will take some planning, but it offers a simple method to quickly check the transceivers on the GTP that will be running on an Altera device.
→Continue with firmware development for the initial acceptance testing of the GTP and Ethernet interface. It will be some time before we have a crate full of SSP, so global trigger crate hardware testing will move to the latter part of FY12.

1 July 2011
→No report, but boards are due 6-July. The boards and parts kit will be shipped to the assembly company and the power section will be populated on one board. After the power section has been thoroughly tested, the second board will be approved for full assembly.
→Acceptance test firmware is a work in progress including firmware for the Ethernet section and main GTP functions.

ACTION ITEMS: **Next meeting -Friday 5 Aug @ 10AM in F226**