12GeV Trigger meeting notes:

30 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, E. Jastrzembski, N. Nganga

16 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, J. Wilson

2 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, J. Wilson

19 March 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, J. Wilson, A. Somov

Updated prototype board status table:--21 April 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Daq Lab F110** **EEL – 126** **EEL109** **F-Wing Lab** **Hall A** **EEL – 126**	 **Test Board** **OK Hall A Student** **Moller Spare** **FDC test setup** **Needs repair** **F117 (A. Somov)** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded** **Sent to IU for FCAL testing** **12Oct2009** **'64x crate and LinuX Cpu sent 24Jan10**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Testing complete**

0. Trigger/Clock/Sync – TI/TD

30 April 2010

-->William is close to the final steps of preparing the TI-TD board for order. Ben and others have reviewed the schematic and it would be prudent to check the fabrication files before sending to the selected manufacturer. Components will be ordered with the DAQ account for at least two modules.

--> There was some discussion regarding the function of the TI and if the firmware would support a bus master option. William has started the firmware development, and presumably existing VHDL code blocks can be reused from other designs where applicable.

16 April 2010

William is at the stage of final checking for the layout of the new TI-TD module. The schematics should also be closely checked, and William has created a detailed Bill Of Materials. The initial manufacturing and assembly of the board will be funded from the DAQ group and the FPGAs required for the initial boards have already been purchased from PELEC funds.

William and Ben compared the jitter between two Avago fiber transceivers and the results were virtually identical. The 2.7Gbps part will be used for the TD-TI links and the higher speed transceiver will be used for the CTP-SSP links.

Fiber transceivers for full testing of the TI-TD will need to be ordered, and we will order at least 6 of the higher speed transceivers for the SSP testing.

William has made progress on two other designs in parallel with the high priority TI-TD project. The fanout module for the CAEN V1290 TDC has been defined and is progressing, plus the mezzanine card adapter for the TI-TD is also in progress.

William has provided updates to the schedule for three board projects. The TI/TD module design is progressing nicely and schematics are ready for a check.

The 2.7Gbps transceivers were received and were tested in the lab by Ben and William. Results were not remarkable compared to the 3.125Gbps transceivers, but a few plots of the results would be useful. These components would save some costs for the TI-TD fiber links.

As soon as a BOM is created for the prototype TI/TD, any long lead items should be ordered.

1. FIRMWARE TESTING

30 April 2010

-->Dave Abbott has implemented the new playback mode to the existing FADC250 library. There has also been work effort to allow for more points for each of the playback channels. A method to implement more points for each of the 16 playback channels has been discussed (implemented?) so that the Xilinx memory cell usage is optimized.

-->Alex continues to test the playback features and the next steps may be to discuss how the CTP will need to be configured and operated when in playback mode. Simple summing can be used, but there may be other modes for the CTP configuration in the 'playback' mode. Further discussions will be necessary.

16 April 2010

→A few iterations to the Playback mode have been completed, and Dave Abbott has started to add the new “Playback” mode to his existing FADC250 library. These functions will be eventually used for system commissioning and test. This “Playback” feature will be very useful to test and troubleshoot the entire trigger system. It might be a good time to draft a full description of this “Playback” mode including an implementation plan.

→PREx is off to a successful start and the Moller firmware has been in use for some time now. It would be interesting to see the results from the experiment data.

→Firmware design and testing is close to completion for Ed’s full conversion of the AHDL to VHDL for use on the latest revision of the FADC250 and this firmware can be used for future VME module designs.

2. *SUB-SYSTEM PROCESSOR (SSP)*

30 April 2010

-->Ben has only a few minor items to address on the final board manufacturing files and the SSP is ready for order!! Another milestone passed!

-->Firmware for the SSP has been developed and the latest in firmware simulation tools has been purchased by the Hall B group. The new tools will allow simulation of multi-board interaction and allow for fast iterations of code testing. Test code to simulate the trigger data transfer between CTP and SSP is a prime example, and any new or required error detection methods can be simulated and tested.

16 April 2010

→The SSP is at the stage of checking manufacturing files and final review of all schematic and design rule checking. Considering the complexity of this board and the number of layers, it is prudent to verify and check the design before ordering the initial board. No significant issues to

report here regarding the Altium –to- Cadence Specctra routing, and Ben has provided a significant amount of work to keep this project on schedule.
→All components for the initial SSP have been ordered. We will order the fiber transceivers soon.

3. CUSTOMERS

30 April 2010
No new items to present other than the property transfer of a 12 slot VXS crate and flash board have been transferred to the Injector group. They will use the flash board and trigger features to readout a new polarimeter design including the existing Mott polarimeter. They have committed $10K for two Rev-1 FADC250.

16 April 2010
→PREx in Hall A is running!
→IU FCAL group is finished with the 12 bit FADC250. Not sure if they will send that unit back to Jlab soon, but the last email I read indicated that they had collected plenty of data with the new timing algorithm and have produced a paper with the results.
→One FADC250 has been reserved for the JLAB Injector group for their upcoming Compton and Mott applications. They will need a test crate and supporting peripheral level translator for the trigger input, and the hardware has not yet been transferred to them. Contact: Joe Grames
→Table 1 has been updated and the 9 prototype FADC250 units have been stable and in use for close to a year without significant problems.

4 "B" Switch - Signal Distribution Module (SD)

30 April 2010
--> Nick and Mark will begin the ECOs for the SD module and prepare the board for its final revision. The prototype SD boards were designed with PCAD and have been converted to Altium. All modifications will be completed using Altium for the final revision.

The most significant design changes are the new pair mapping for the SD signals, and the addition of a dedicated pair to the TI module to support a high speed link for diagnostic and scaler event data.

16 April 2010
→**Welcome to Nicholas Nganga!** Nick has started work and will be assigned to the revision of the SD module. Other projects will be assigned as well, but for now, he will be ramping up his understanding of our trigger system architecture and design specifications for the SD module.
→The final VXS pair mapping has been defined for the front end and global trigger crates. The final mapping definitions have been revised on the FADC250-V2 and of course, the new trigger module designs will use this final pair mapping.

5. System Diagrams & Test Stand Activities

30 April 2010
--> We had a good discussion regarding the need to start the development of libraries for the CTP and other boards in the 12GeV trigger system. We are about five months away from FY2011 and the number of new boards to test in a full system test with CODA is approaching. The following list highlights the library status and offers a glimpse of what effort is needed to complete the driver libraries.

- FADC250 Rev-1 Virtually the same library as what exists now. There are many features, modes that have been added over the years and these will need full functional testing.

- FADC125 Rev- The prototypes have been delivered for these boards and even though they are not included as input to the trigger system, I list the board here because the library development will have to start soon and continue into FY11.
- CTP Rev- Two prototypes completed over a year ago, and library development has started. Implement I^2C communication via TI and other functions.
- TI-TD Rev-1 Prototypes of the final revision will be produced soon. Specification for features and functions needs to be updated, and register map developed. Many functions will remain the same as the initial prototypes, but there are significant hardware features that will need to be considered for the CODA library driver.
- SD Rev- Two prototypes were completed over a year ago, and the driver library could be started in concert with the CTP development because the communication link is the same. The features and register map for the SD are not numerous, so this could be completed before end of FY10
- SSP Rev- Initial prototype to be fabricated and assembled by July. Plenty of board level testing before library development can begin.
- GTP Rev- Definitely a FY2011 activity
- F1TDC Rev-2 Definitely a FY2011 activity, and the good news is that the existing firmware and driver provide a significant boost to the development stage.
- TS Rev-2 FY2011 or FY2012?

16 April 2010

The time has arrived to discuss the testing activities for the SSP, TI-TD and other system level testing that will be required after these modules have been received from assembly. Many of the test activities will be low level board functionality tests, which will require test crates, and other support hardware.

The activities for developing libraries for CODA will have to be accounted and I believe we should plan for FY11 to implement the next level of 'DAQ System' testing that will be required to test and measure the performance of the readout and trigger hardware in a multi-crate format. We have performed these tests with the ***prototypes*** of the FADC250, CTP, SD and TI and the next level of testing will include more FADC250, SSP and the new TI-TD. I would like to dedicate some time to discuss these activities at the 23-April meeting.

Crate Trigger Processor (CTP)

CTP activities are complete. (CODA library 'driver' has started)

6. Projects for FY10

16 April 2010

→No action on the GTP other than an update to the specification and selection of the Xilinx FPGA.

→Details of the testing activities will need to be listed soon, as I suspect there will be a need to order a few essential items to support these new system level tests

→No action on updating the trigger system diagrams for the fiber optic distribution. These drawings must be completed in FY11 and all cable and fiber hardware specified for procurement.

→Full crate test activities need to be detailed

ACTION ITEMS: **Next meeting → Friday 7 MAY 2010 at 10:00am in F228**