12GeV Trigger meeting notes:

1 April 2011: C. Cuevas, B. Raydo, N. Nganga,. E. Jastrzembski, B. Moffitt, H. Dong,S. Kaneta, J. Gu; A. Somov, J. Wilson

25 March 2011: C. Cuevas, B. Raydo, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov, J. Wilson

18 March 2011: C. Cuevas, B. Raydo, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov

11 March 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J.Wilson, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov

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0. Trigger/Clock/Sync – TI/TD

1 April 2011

A TID and SD have been installed the EEL109 VXS DAq crate. A 150m fiber has been connected from TI-port 5 to TI-port 1 through the patch panel and fiber patch cords. The number of tests that can be performed with these two boards is not too large, and a payload test board can be used to monitor clocks and other signals that are driven by the SD board. The status of the firmware for the TI and SD is complete for now, and Bryan can continue testing the library functions for each of these boards.

25March2011

TID is ready to be installed in EEL109 test rack. William has updated the TI-D manual and has included detailed explanation of the fiber skew offset and compensation 'procedure' to maintain zero skew between each front end crate. The skew can be controlled to 4ns.
Latest manual has been updated and posted. Pre-production parts will need to be ordered, and also order for front panels can be released.

18 March 2011

William has completed the ECOs from the initial version of the TI-D. A pre-production order will be placed after successful two crate testing in May-June. Component and front panels can proceed to procurement for the pre-production batch of ten or twelve TI-D units. Not sure how many of these versions will be used in full distribution mode, but further testing can be completed when the pre-production versions are received.

At least one TI-D will be installed in EEL109 crate by Tues 22-March. Proceed to connect/configure first crate with 50m fiber and patch cables, along with a SD module.

4 March 2011

A brief discussion on radiation affects on the Avago transceivers was opened by Chris and there are several articles from LHC groups that cover not only the electro-optics, but the fiber degradation from radiation dose. Fortunately there will not be high enough radiation dose in Halls D & B, and the equipment racks will be a decent distance from the Tagger and Target areas. At any rate, if someone would like to research this topic further we can discuss this again and possibly set up a test in Hall C or Hall A. Avago does not have radiation affect data for their fiber optic transceiver product.

William brought up the point about the CLKA and CLKB signals that the TI-D will distribute to the SD. The present design revision does not allow any of the three clock choices to be distributed to either CLKA or CLKB. The SD provides fan-out of CLKA to the "odd" payload ports (Left) and CLKB to the "even" payload ports (Right). The final TI-D requirement is to send any of the three clocks (250MHz, 125MHz, and 31.25MHz) to both CLKA and CLKB. (D. Abbott)

2. *SUB-SYSTEM PROCESSOR (SSP)*

1 April 2011

Ben reported that he is at the stage of reviewing the details of the transmission protocol/scheme for the link between the CTP and the SSP. 4 bonded Aurora lanes @2.5Gp/s was the method used in 2009, and this will have to be reviewed. Hai will be ready to work with Ben on the CTP->SSP link firmware after work for the FADC250 is running flawlessly.

25 March 2011

No report

18 March 2011

Some discussion on how the SSP will be used in the two crate DAq test. Register map, configuration, summing function, etc need to be defined and Bryan can start the driver routines. Ben mentions that he will need to discuss the transmission protocol definitions with Hai so that any firmware that needs to be written and tested for the CTP->SSP fiber link can proceed. The SSP will be used to combine the trigger data from two CTP and send the trigger to the TI-D (TS mode)

4 March 2011

Ben reports that the testing of the SSP is complete and that he will spend some time on the firmware required for the SSP in the two crate DAq setup. The SSP is planned to be used to collect the trigger data from two CTP and combine this trigger information and create the L1 trigger signal that will be sent to the TI-D. At some point soon, the CODA 'driver' library for the SSP will have to be created, so whenever the firmware is at a stable revision, Bryan can start the library development.

3. CUSTOMERS

1 April 2011 (Not an April Fools)

Ed reports that the FADC250 board has been tested and that the data format and other firmware features are working. Hopefully we can use at least one of the version 2 boards for initial testing with the SD, TI and CTP in the EEL109 DAq crate. The FADC250-V2 that was loaned to the Radiation Detector and Imaging group should be returned and loaded with the latest firmware so that we can begin populating the 2nd DAq crate.

25 March 2011

Breakthrough on testing and troubleshooting located the firmware issues. Further testing continues. Boards ordered, assembly needs signature from HallB. Secondary order is progressing, need to check parts kit.

18 March 2011

Ed reports that the testing of the FADC250-V2 is in the final stage. The circuit board order has been placed, and the assembly procurement has been placed. There is a separate assembly order for the medical imaging and injector group boards, and virtually all the components for this secondary assembly order have been received.

4 March 2011

I will keep this section to list a brief status of the FADC250 boards, and Ed reports that testing with the version 2 pre-production unit is going well and that 2eSST readout is imminent. The order for 35 boards/assembly is ready to proceed.

4 "B" Switch - Signal Distribution Module (SD)

1 April 2011

For the time without a FADC250-V2 board, we can use the payload test board to send a trigger signal to the SD and pass this signal to the TI. Nick has been busy with final firmware changes and has also started to implement the ECOs for the final board design. The components for six SD boards have been received and assembly of the parts kit has started. Soon after the two crate DAq testing, we can send the order for a six board assemblies. The front panel drawings should be checked and ordered now.

25 March 2011

It all works! BUSY discussion and details of other functions need to be coded.
Token
Busy
I^2C working
PLL working
SD-TI "link"
Trigger Hit Pattern block
Counters (Scaling various signals)

18 March 2011

Nick reports that he is in the process of finalizing the SD firmware. Hardware testing of all the I/O for the SD board with the latest firmware is cumbersome because the SD receives signals from every payload module. Token passing, Trigger_Out and Busy are examples of signals that need to be verified. Essential firmware for I^2C processing and controlling the PLL appears to be completed.
Nick has maintained the ECO list accuracy, but these changes have not been implemented in the schematic or the revision layout. There are already components for at least six more SD, and the front panels can be ordered now for the pre-production lot.

The test plan is to move at least one SD module to EEL109 crate by 23-March. This SD can be tested with Bryan's latest driver library and the TI-D.

4 March 2011

Nick presented a block diagram of the test setup used to perform the clock distribution jitter analysis. He showed how the use of an external receiver/buffer circuit allowed a precise baseline measurement of the test equipment. The 250MHz clock was distributed from the TI-D to the SD and the clock signal was measured at PayloadPort-15. The jitter was measured with and without the SD jitter attenuation PLL circuit and the results showed that the PLL circuit worked as designed. The baseline jitter 'calibration' was a very good method and demonstrated that the PLL jitter contribution is negligible.

5. System Diagrams & Test Stand Activities

1-April 2011

Start a pre procurement plan for Hall D to include fiber trunk installation and testing. Patch cables and patch panels will be ordered separately.

25 March 2011

Re-work the price estimate for only installation and cost of the 144 fiber trunk lines.

18 March 2011

The initial price quote received for the MTP trunk Fiber and supporting peripheral hardware is surprisingly high. The company included assembly, installation and testing of the MTP trunk

fiber cabling for the Hall D example. The company assumed that the trunk cables would be all the same length, but in fact the trunk cables for the Hall will be much shorter, so the cost would also be reduced significantly. On further review, the jacket of the trunk and patch cables can be rated lower than plenum or riser, and this specification will reduce the overall cost further. All said, another price estimate will be generated.

4 March 2011

A brief discussion on the collection of hardware that has been assembled in EEL109 for the two crate DAq test. In the next week or two it would be an important goal to setup a single crate with a CPU, TI-D, CTP, SD and a single FADC250. There are numerous details to verify a 'simple' configuration of these essential modules.

The price estimates for the trigger system fiber optic cabling, patch panel hardware and installation is due this week from the initial vendor. There are quite a few details to discuss before installation in the hall.

5. Two Crate DAq test configuration

1 April 2011

TI-D, SD, Linux ROC, are **installed in the EEL109 lab!!** 150m fiber with patch panels installed also. We will need a FADC250-V2 as soon as possible**!** At least one FADC250-V2 will be ready by 15-April!

The clock phase alignment procedure has been completed by William, and the adjustment for clock phase alignment between front end crates is one 4ns clock cycle.

25 March 2011 (This is in red because we missed the goal!)

Major components for the two crate DAq test are installed in EEL-109. Still need another VXS crate, and the boards will have to have the latest firmware revisions loaded and ready.

*We plan to have at least one crate running with the CPU, TI-D, SD and CTP **by next meeting**. If we can get one of the FADC250-V2 boards, that would be a bonus*.

18 March 2011

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We plan to have at least one crate running with the CPU, TI-D, SD and CTP by next meeting. If we can get one of the FADC250-V2 boards, that would be a bonus.

11 February 2011

We had a significant discussion about the two crate Daq/Trigger testing that will happen in a few more months once the pre-production lot of FADC250 arrive. In the meantime, we have a virtually all the other hardware needed for this test. See below:

Description	Quantity	Firmware Rev	Model#	Notes
VXS Crate	2	n/a	Wiener	EEL-109/Chris
Single Board CPU	2	Linux ?	?	Bryan/Dave
CTP	2	?	Use latest version	Hai/Scott
SD	2	?	Use Rev1 boards	Nick
TI-D	2	?	1-TI 1-TI-D	William
SSP	1	?	Prototype	Ben
Fiber	2 -50m & 150m	n/a		EEL-109
Fiber patch	1	n/a		EEL-109
Fiber patch cables	4	n/a		EEL-109

For the DAQ/CODA software side:

Description	Quantity	Revision	Model#	Notes
GigEthernet Switch	1 multi port			EEL-109
Linux PC	1	Dell 1U	FAST	Installed by Bryan in EEL109
CODA				Bryan/Dave
CODA board libraries				Bryan/Dave

We have test equipment, pulsers, fan-out modules etc so that should not be an issue.
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of readout rates, trigger rates, and a variety of other information needed to claim success.
The list of verification requirements (goals) are listed below:
→**Goals of the integration testing**:
-Verify clock distribution through TID-SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

   The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

   Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

1 April 2011

→CTP 1 and 2 will be used *initially* in the two crate test. These units use LX110T and will have the transceiver selection *hardcoded* in the FPGA for a single FADC250.

→For the **final** two crate configuration with 16 payloads we will use CTP 3 & 4 that are assembled with the FX70T part. We will need to have the CTP firmware developed so that each of the Gigabit transceivers can be disabled or enabled. If there are counters (scalers) that need to be added, these must be defined now.

→The ECO list for the CTP design is well known, and will need time to implement on the schematics and PCB. These changes include adding front panel I/O and other small circuit corrections. These ECO are in the plan and create a good deal of work to complete before the end of fy11.

25 March 2011

Let's talk with Hai to verify the next step. The latest CTP have V5FX70 parts and the full firmware needs to be loaded into the latest CTP. There are a few functions that need to be added so that the CTP 'lanes' can be enabled/disabled for the full crate test.

What other essential counter functions will be required?

18 March 2011

Two CTP repaired and Scott has verified clock works properly. Hai has implemented at least one of the original two boards with the full code and new I^2C block. At least one of these CTP can be installed in the EEL109 crate.

CTP to SSP link definitions need to be reviewed and completed in the not too distant future. Firmware will have to be revived and updated to control/interface up to sixteen FADC250 boards also. The two crate test completed in spring 2009 used a CTP that was coded for specific payload slots.

4 March 2011

The two newer CTP units have been received from the rework vendor, and the repairs appear to be OK. At least two of the four CTP units will have to be loaded with the final firmware revision soon which includes the latest I^2C block from Nick. Need to push this to a higher priority soon.

7. GTP and Global Crate Developments

1 April 2011

Scott presented the latest update on the board layout and the routing for the transceiver lanes look very impressive and on one layer and manage sixteen SSP with 2 full duplex lanes! The board routing paths for the memories, and Ethernet interface is a work in progress. The Specctra router routines will need to be developed but the progress is very promising. Ethernet firmware and Nios embedded code will begin when board sent for assembly. Initial code framework has been developed.

25 March 2011

GTP 3D video of an Altium layout

18 March 2011

Scott has started the board layout process and showed the most recent board with the major component placement. The power section and bypass capacitor analysis has been completed and the power plane sections have been defined on the board. Scott has recently attended a signal integrity seminar, and is gaining valuable experience with this GTP project. A review of the schedule looks OK, and progress is converging toward the scheduled goals.

4 March 2011

Scott, Nick, Ben, Hai and Chris met after the trigger meeting to review the latest GTP schematic. This 'review' was helpful and no show stoppers were identified. There were several important details that were noted, and Scott captured the changes that need to be added. Board layout should begin as soon as possible.

ACTION ITEMS: **Next meeting → Friday 8 April 2011 10AM in F226**