12GeV Trigger meeting notes:

28-May 2010: C. Cuevas, H. Dong, B. Raydo, A. Somov, E. Jastrzembski, N. Nganga,

21 May 2010: No Meeting

14 May 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, E. Jastrzembski, J. Wilson, G. Visser, D. Abbott, F. Barbosa, B. Zihlmann, L. Pentchev

7 May 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, E. Jastrzembski, N. Nganga, J. Wilson

30 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, E. Jastrzembski, N. Nganga

Updated prototype board status table:--21 May 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Injector Group** **EEL – 126** **EEL109** **F-Wing Lab** **Hall A** **EEL – 126**	 **Test Board** **Moller Spare** **Injector Group** **FDC test setup** **Needs repair** **F117 (A. Somov)** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded** **Sent to IU for FCAL testing** **12Oct2009** **'64x crate and LinuX Cpu sent 24Jan10**
4	**Trigger Interface** **Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** Front Panel – Signal Distribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**F-Wing F110**	**CODA Library development**
1	**Crate Trigger Processor**	**F-Wing(Hai)**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**F-Wing F110**	**CODA Library development**

0. Trigger/Clock/Sync – TI/TD

28 May 2010

Ed and Ben will talk with William regarding any corrections to the TID schematic or board layout. William is prepared to send the TID data to the board manufacturer as soon as any last minute changes are complete.

Virtually all components have been ordered and received for the TID. I believe we will manufacture several circuit boards and assemble only one unit for testing.

Not too soon to finish a prototype front panel design and this should be ready by the time testing begins.

➔ The VME front panel clock/trig distribution board is almost completely assembled except for a few parts.

21 May 2010

- ➔ Final check of schematic and Gerber files are almost complete. Board should be ordered before end of May. Virtually all components have been ordered. Quotations for assembly should be started now.
- ➔ Several VME-Front Panel signal distribution cards have been ordered and at least two modules will be assembled to support requests for the use of the prototype FADC-250 boards. Jeff has been assembling these when he has time.

7 May 2010

- ➔ TI-TD board is ready for ordering and the FPGA components have been received for this board and the FADC250-V2.
- ➔ Latest layout and block diagrams presented at the Hall D collaboration meeting

30 April 2010

-->William is close to the final steps of preparing the TI-TD board for order. Ben and others have reviewed the schematic and it would be prudent to check the fabrication files before sending to the selected manufacturer. Components will be ordered with the DAQ account for at least two modules.

--> There was some discussion regarding the function of the TI and if the firmware would support a bus master option. William has started the firmware development, and presumably existing VHDL code blocks can be reused from other designs where applicable.

1. FIRMWARE TESTING

28 May 2010

→ Alex and Hai discussed the details of how to implement (and optimize) the available RAM that is available in the front end FPGA. The method will use enough points for at least a 100nS pulse (25 points).

→Test work continues in the F117 lab with the FADC250 setup and the new firmware to support the new playback method is not complete. I believe Dave's library will have to also be updated after Hai has tested the latest playback firmware.

→William was not present, but a discussion about the firmware development plan for the new TID was started. VHDL is the 'standard' and it certainly makes sense to use this standard for developing firmware. It will make development of test benches easier, and many firmware blocks can be re-used from other projects. At the next meeting we should discuss the outline of a firmware development plan for the new TID.

21 May 2010

No update on the implementation of the new 'playback' mode that will support the addition of more waveform points for each channel. Alex presented the highlights of the 'playback' mode at the recent Hall D collaboration and showed how this new mode will be put to use during the commissioning period and for system level troubleshooting.

No update on the firmware implementation for the new TI-TD module. Presumably many of the functions used on the prototype revision can be used on the new module.

7 May 2010

The new method to create more points for each of the playback channels has been simulated by Hai, but not implemented in the hardware yet. The library that Dave A. created to support the existing playback mode will need to be updated once the new firmware has been tested.

Alex continues testing and implementing new ideas for the playback mode and presented methods to use this technique for commissioning the DAQ and trigger systems in the halls.

30 April 2010

-->Dave Abbott has implemented the new playback mode to the existing FADC250 library. There has also been work effort to allow for more points for each of the playback channels. A

method to implement more points for each of the 16 playback channels has been discussed (implemented?) so that the Xilinx memory cell usage is optimized.
-->Alex continues to test the playback features and the next steps may be to discuss how the CTP will need to be configured and operated when in playback mode. Simple summing can be used, but there may be other modes for the CTP configuration in the 'playback' mode. Further discussions will be necessary.

2. ***SUB-SYSTEM PROCESSOR (SSP)***

28 May 2010
→SSP boards should be here next week and the assembly quotations should also be received next week. There are a few details that the assembly vendor has identified and these will be addressed in their assembly quote. I believe all the parts are in a kit, and ready to be sent once the PO has been created for assembly. Is the front panel ready for machining?

21 May 2010
→The SSP has been ordered with a ten day delivery. All the components for one module have been received, and the order for assembly will need to be submitted soon.
→This would be a good time to discuss/document a test plan for the SSP.

30 April 2010
-->Ben has only a few minor items to address on the final board manufacturing files and the SSP is ready for order!! Another milestone passed!
-->Firmware for the SSP has been developed and the latest in firmware simulation tools has been purchased by the Hall B group. The new tools will allow simulation of multi-board interaction and allow for fast iterations of code testing. Test code to simulate the trigger data transfer between CTP and SSP is a prime example, and any new or required error detection methods can be simulated and tested.

3. CUSTOMERS

21 May 2010
No update other than FADC250-SN003 has been transferred to the injector group for their new polarimeter development. A VME front panel signal distribution module will also be given to them once the unit is assembled and tested.

30 April 2010
No new items to present other than the property transfer of a 12 slot VXS crate and flash board have been transferred to the Injector group. They will use the flash board and trigger features to readout a new polarimeter design including the existing Mott polarimeter. They have committed $10K for two Rev-1 FADC250.

4 "B" Switch - Signal Distribution Module (SD)

28 May 2010
→Nick continues with the revisions to the SD board and we had a good discussion about adding a jitter attenuation part to the SD for both the 'right' and 'left' clocks that are received from the TI board. The component that is strongly suggested is the SiLabs part that contains an on board VCO and small footprint for a dual channel device. Test results show that this component will reduce the jitter from the long fiber runs and is the best location to drive all the boards in a crate. There was also a discussion regarding any other implications of introducing a PLL device at the SD, for instance, will synchronizing the boards be an issue? Stay tuned,,

21 May 2010

→Nick has created a list of the changes to the SD pair mapping and will include these changes to the revision design. The pair mapping changes will have to be made on the existing SD units to support testing of other modules. There may be enough time to finish the revisions to the existing design and possibly order the Rev-1 board by end of the fiscal year, but it is an aggressive plan.

→The discussion about adding an alternate data readout path from the SD have been noted from previous meetings, but there are significant details to the design that have not been discussed. I know this alternate data path is not a requirement, but it would be useful. The present implementation plan is to use a single pair 'link' from each payload slot to the SD switch slot. There is a single pair 'link' to the TI board but it is not clear what data will be sent to the TI through this path, as it does not offer alternate data path because the TI is readout through VME.

30 April 2010

--> Nick and Mark will begin the ECOs for the SD module and prepare the board for its final revision. The prototype SD boards were designed with PCAD and have been converted to Altium. All modifications will be completed using Altium for the final revision.

The most significant design changes are the new pair mapping for the SD signals, and the addition of a dedicated pair to the TI module to support a high speed link for diagnostic and scaler event data.

16 April 2010

→**Welcome to Nicholas Nganga!** Nick has started work and will be assigned to the revision of the SD module. Other projects will be assigned as well, but for now, he will be ramping up his understanding of our trigger system architecture and design specifications for the SD module.

→The final VXS pair mapping has been defined for the front end and global trigger crates. The final mapping definitions have been revised on the FADC250-V2 and of course, the new trigger module designs will use this final pair mapping.

5. System Diagrams & Test Stand Activities

28 May 2010

→No new updates and there was some email traffic regarding the initial "CODA-Driver" for the FADC125. Presumably this work has been completed or a new plan established to complete the required readout software test plan.

→Must continue with updating the overall fiber distribution diagrams so that preliminary estimates and specifications can be started for the procurement of all the fiber needed for the trigger/clock/sync distribution network. These estimates and specifications will include the required hardware for patch panels and patch cabling. Will also need to verify the lengths between racks and the main trigger modules.

→Crate procurement activity is going well. Nothing new to report and sources have submitted information for evaluation.

14 May 2010

Gerard Visser has delivered the first 72 channel FADC125 and it is connected to the FDC full scale prototype in the EEL 126 lab. Gerard presented the details about how the data is collected and controlled on the new board and showed the stages of his initial software to readout the data.

The discussion continued about the existing implementation of readout functions and mentions of what other types of algorithms/functions are planned for the FADC125. The present modules

do not use the VXS path for trigger and other common signals, and Gerard is aware of the signal pair modifications.

Additional information was presented on the (CODA) library development plan including event blocking details.
What are the work (activities) needed for the next six months?

- ➔ Now working in lock step readout 'mode' – 1 trigger, readout channels, done
- ➔ Implementation of block trigger pipeline mode will be next activity. Coordinate with Daq group, share firmware?
- ➔ Implement other algorithms and test trigger rate capabilities
- ➔ Hardware changes → P0 remap; and any other minor ECOs will need to be completed.
- ➔ COOLING ISSUES: We will have to verify the air flow requirements to cool a full crate of front end modules including the switch slots and CPU module load. Preliminary measurements in the 'standard' Wiener crate shows airflow lower than needed, and we will most likely need to change the airflow requirement to fit the higher power dissipation of the front end cards.

30 April 2010

--> We had a good discussion regarding the need to start the development of libraries for the CTP and other boards in the 12GeV trigger system. We are about five months away from FY2011 and the number of new boards to test in a full system test with CODA is approaching. The following list highlights the library status and offers a glimpse of what effort is needed to complete the driver libraries.

- FADC250 Rev-1 Virtually the same library as what exists now. There are many features, modes that have been added over the years and these will need full functional testing.
- FADC125 Rev- The prototypes have been delivered for these boards and even though they are not included as input to the trigger system, I list the board here because the library development will have to start soon and continue into FY11.
- CTP Rev- Two prototypes completed over a year ago, and library development has started. Implement I^2C communication via TI and other functions.
- TI-TD Rev-1 Prototypes of the final revision will be produced soon. Specification for features and functions needs to be updated, and register map developed. Many functions will remain the same as the initial prototypes, but there are significant hardware features that will need to be considered for the CODA library driver.
- SD Rev- Two prototypes were completed over a year ago, and the driver library could be started in concert with the CTP development because the communication link is the same. The features and register map for the SD are not numerous, so this could be completed before end of FY10
- SSP Rev- Initial prototype to be fabricated and assembled by July. Plenty of board level testing before library development can begin.
- GTP Rev- Definitely a FY2011 activity
- F1TDC Rev-2 Definitely a FY2011 activity and the good news is that the existing firmware and driver provide a significant boost to the development stage.
- TS Rev-2 FY2011 or FY2012?

Crate Trigger Processor (CTP)

28 May 2010

→Bryan and Dave have the switch cards and a full sized VXS crate in the F110 Daq lab to begin the development of software to control the CTP and SD boards from the TI. These modules will definitely be revised, and the iteration of the software will go through a few revisions too. Before too long, it might be a good idea to review the specifications of each module and finalize the control and readout register map.

21 May 2010

At least one CTP is in the DAQ lab including a full 21 slot Wiener crate and prototype TI so that a library can be developed to support the CTP and SD functions.

CTP activities are complete for FY10

6. Projects for FY10

16 April 2010

→No action on the GTP other than an update to the specification and selection of the Xilinx FPGA.
→Details of the testing activities will need to be listed soon, as I suspect there will be a need to order a few essential items to support these new system level tests
→No action on updating the trigger system diagrams for the fiber optic distribution. These drawings must be completed in FY11 and all cable and fiber hardware specified for procurement.
→Full crate test activities need to be detailed

7. ***Global Trigger Processor(GTP)***
   →The start of the schematic is official and I have created a new project with Altium and started the schematic. It was a significant time saver to use the CTP design directory and files that were created with PCAD because the GTP is also a switch card format.
   →A bit behind schedule, but with some help I believe an initial layout can be realized before the end of the fiscal year.

ACTION ITEMS: **Next meeting → Friday 4 JUNE 2010 at 10:00am in F228**