

12GeV Trigger meeting notes:

16 July 2010: C. Cuevas, H. Dong, A. Somov, N. Nganga, W. Gu, J. Wilson, B. Mofitt, F. Barbosa, E. Smith, D. Abbott

8 July 2010 – 12GeV Trigger Workshop @CNU

4 & 11 June 2010: C. Cuevas, H. Dong, B. Raydo, A. Somov, E. Jastrzembski, N. Nganga, W. Gu, J. Wilson

Updated prototype board status table:--19July 2010 **No changes**

Quantity	Description	Location	STATUS/Contact
8	10 bit FADC250 SN001 ----- SN002 ----- SN003 ----- SN004 ----- SN005 ----- SN006 ----- SN007 ----- SN008 -----	Daq Lab F110 Daq LabF110 Injector Group EEL – 126 EEL109 F-Wing Lab Hall A EEL – 126	Test Board Moller Spare Injector Group FDC test setup Needs repair F117 (A. Somov) Moller setup FDC test setup
1	12bit FADC250	Indiana Univ	New timing algorithm firmware loaded Sent to IU for FCAL testing 12Oct2009 '64x crate and Linux Cpu sent 24Jan10
4	Trigger Interface Trigger Distribution	EEL109/DAQ Lab	Modules used for system testing
5	VME -- FP-SD Front Panel – Signal Distribution	EEL109/DAQ Lab	Complete Use in test crates
1	Crate Trigger Processor	F-Wing F110	CODA Library development
1	Crate Trigger Processor	F-Wing(Hai)	Successful testing with multiple FADC250 and in SSP mode!!
2	Signal Distribution	F-Wing F110	CODA Library development

0. Trigger/Clock/Sync – TI/TD

16 July 2010

The new TI-TD boards have been received from the assembler. They certainly look fine and William has started a test plan and will need a dedicated Jtag programmer to begin the firmware development process. The front panels have been received also. Schedule shows plenty of time allocated for complete testing of the prototype module.

11 June 2010

→TID board and components have been ordered! Delivery of two weeks for 2 boards and assembly quotations have been received also. Should have fully assembled prototype by mid July. Would be a good time to finalize the front panel drawing and submit a job for the metal fabrication.

→Jeff and Armen are building up a few more VME front panel clock/trigger distribution modules to support test setups and for the injector polarimeter folks.

1. FIRMWARE TESTING

16 July 2010

Bryan and Dave report that the CTP and SD Coda Library development is going to progress once the new TI-TD has been tested. The implementation of the I²C is significantly different than the initial TI prototype, so waiting for the new TI-TD to be tested makes sense.

Two VME64X crates have been rebuilt using ELMA 20 slot VXS backplanes. These new crates are in the DAQ lab.

11 June 2010

→Hai has delivered the latest update for the "Playback" mode. The latest optimization will allow for 32 points per channel. This will allow for a 128ns playback window where Users can load a single pulse or multiple pulses. The latest firmware has only been added to one of the prototype FADC250 modules and Alex continues with testing.

→Bryan Moffit has been developing libraries for the SD and CTP modules. No update on progress but he is using a full size VXS crate for his testing needs. We have new 20 slot ELMA backplanes and we will change out a few '64x backplanes as time permits.

28 May 2010

→ Alex and Hai discussed the details of how to implement (and optimize) the available RAM that is available in the front end FPGA. The method will use enough points for at least a 100nS pulse (25 points).

→Test work continues in the F117 lab with the FADC250 setup and the new firmware to support the new playback method is not complete. I believe Dave's library will have to also be updated after Hai has tested the latest playback firmware.

→William was not present, but a discussion about the firmware development plan for the new TID was started. VHDL is the 'standard' and it certainly makes sense to use this standard for developing firmware. It will make development of test benches easier, and many firmware blocks can be re-used from other projects. At the next meeting we should discuss the outline of a firmware development plan for the new TID.

2. SUB-SYSTEM PROCESSOR (SSP)

16 July 2010

No report from Ben today, but the board has been shipped and should be here on Monday. I saw the board this morning (Mon 19July) and it looks very good and there will be plenty of testing to start. I know we have the required number of fiber transceivers for both the SSP and TI-TD and we also have on order several of the fiber cables we will need to complete loop back testing as well as board to board testing.

11 June 2010

→The bare SSP boards have been received and it looks like ACE did a fine job. One small detail is that the vias in the BGA areas need to be covered with mask. This was specified and ACE will take care of this issue before the board is sent to the assembler. The assembler has all the components and will complete the assembly with a 10 day delivery. Should have the SSP ready for testing by mid-July!

28 May 2010

→SSP boards should be here next week and the assembly quotations should also be received next week. There are a few details that the assembly vendor has identified and these will be addressed in their assembly quote. I believe all the parts are in a kit, and ready to be sent once the PO has been created for assembly. Is the front panel ready for machining?

21 May 2010

→The SSP has been ordered with a ten day delivery. All the components for one module have been received, and the order for assembly will need to be submitted soon.

→This would be a good time to discuss/document a test plan for the SSP.

3. CUSTOMERS

11 June 2010

No new requests. There have been a few requests for support of the FADC-125 but no new customer requests to report.

21 May 2010

No update other than FADC250-SN003 has been transferred to the injector group for their new polarimeter development. A VME front panel signal distribution module will also be given to them once the unit is assembled and tested.

4 "B" Switch - Signal Distribution Module (SD)

16 July 2010

Nick presented his latest updates and the schematic has been checked by several folks. The clock signals received from the TI will have the capability to pass through a clock jitter attenuation circuit and this has been implemented on the design. The power section has been optimized and significant part reduction has taken place. The placement of the components and pre-route analysis is in progress.

We plan to order at least 4 bare boards and order components for 4 boards. The initial assembly will be for 2 boards and Mark and Nick are preparing the component orders. Now would be a good time to begin the front panel design too.

The discussion about how to implement and optimize the TI-SD link pair and also the Flash-SD link pairs started, and the topic needs a dedicated meeting/discussion to optimize the parameters and limits of these data link connections.

11 June 2010

→Nick has completed the schematic for the SD-Rev1 module. The schematic has been updated to include ECO from the original prototype unit, and the conversion from PCAD to Altium appears to be complete.

→After some discussion, the addition of the SiLabs PLL jitter attenuation part is included on the new revision, the power section has been modified, and a new Altera part has been selected. The schematics are available on the M:drive for review.

5. System Diagrams & Test Stand Activities

16 July 2010

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

- A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
- B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

- A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been

implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

- B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

11 June 2010

→No new updates for system diagram changes, but this will have to be completed in the early months of FY11 so that fiber and support hardware can be specified and purchased.

**** 12GeV Trigger Workshop @CNU on Thursday 8 July, 2010 has been announced ****

Crate Trigger Processor (CTP)

16 July 2010

A brief update regarding the order for two more CTP for Hall B. These parts and boards are in the order process now, and we will build these modules using the V5FX70T parts as a simple "upgrade". The plan is to use these new boards for testing the FADC250 at higher Gigabit transceiver speeds, and also to support the proposed experiment in Hall B planned for September 2011.

11 June 2010

→No update on the success or problems associated with developing driver software libraries for the SD and CTP units. The new TID will arrive soon, so before the end of summer it would be an aggressive goal to have new library support for these modules.

28 May 2010

→Bryan and Dave have the switch cards and a full sized VXS crate in the F110 Daq lab to begin the development of software to control the CTP and SD boards from the TI. These modules will definitely be revised, and the iteration of the software will go through a few revisions too. Before too long, it might be a good idea to review the specifications of each module and finalize the control and readout register map.

21 May 2010

At least one CTP is in the DAQ lab including a full 21 slot Wiener crate and prototype TI so that a library can be developed to support the CTP and SD functions.

6. Projects for FY10

16 July 2010

No significant items to report and the schematic is progressing slowly. The recent addition of the jitter attenuation technique and circuitry that was added to the latest SD revision will be copied to the GTP as well.

11 June 2010

→The GTP Altium schematic has been started and progress is at a glacier pace. (Chris) The proposed Xilinx part exists in the Altium library. The CTP was imported from PCAD to begin the GTP project in Altium and the number of sheets for the GTP should be significantly less than the CTP. Plenty of schematic work needs to be completed. Some of the specifications/requirements need to be documented before the schematic can be completed. The updates to the GTP requirements stem from CLAS12 and the possible need for more than eight (8) SSP in the global crate. Need to build a prototype, and the final version will include the latest requirements.

ACTION ITEMS: Next meeting → Friday 23 JULY 2010 at 10AM in F228