From: Elke-Caroline Aschenauer <elke@jlab.org>

Subject: new sow from sensl

- Date: December 31, 2007 6:59:48 AM GMT-06:00
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 - 🕖 1 Attachment, 287 KB

Dear all,

reading the new proposal from sensl for a SoW for phase II, I see at least 2 big problems.

We don't have \sim 470k\$ for the work proposed neither in the 12GeV and for sure not in the 6GeV Hall D funds.

I actually went also through the statement of work for phase I some of the deliverables sound very similar, but of course no concrete numbers have been given.

I must also admit that I find developing a preamp board for SiPMTs for 71,4 k\$ slightly overpriced. We have the design from Paul Smith, and the one from Sensl Carl uses. This have just to be improved and get the right connectors placed on the board. I think we should be able to do this ourselves.

The other point I'm completely lost is the additional 125k\$ for a circular tile. So is the statement that the CMOS technology used by Sensl allows for monolithic large area SiPMTs not true anymore. This was still stated in the first proposal me got on page 2 under 1.2

I see that we can only do Task 1.1, 1.2 and 2.1 and this has also become 50k\$ more expensive than the original proposal from sensl. Of course this can be due to our changed requirements.

I propose we have a phone conference on this the next days, so we can discuss with sensl our position on this.

Regards and a happy new year Elke

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