Trigger meeting notes:

19 June 09: C. Cuevas, A. Gupta, B. Raydo, M. Taylor; E. Jastrzembski, J. Wilson

12 June 09: C. Cuevas, A. Gupta, B. Raydo, M. Taylor; A. Somov, J. Wilson

5 June 09: C. Cuevas, A. Gupta, B. Raydo, E. Jastrzembski, M. Taylor; A. Somov, J. Wilson

29 May 09: C. Cuevas, A. Gupta, B. Raydo, E. Jastrzembski, F. Barbosa; M. Taylor; A. Somov, J. Wilson

Updated prototype board status table:--*19 June 2009*

Quantity	Description	Location	STATUS
4	**10bit FADC250**	**EEL109/DAQ Lab** **SN002** **SN004** **SN006** **SN008**	**All boards are in use.** **Source Synchronous Transfer (SST)** **4 board test in one crate with Hai's latest firmware. Measure maximum trigger rate.** **Need to modify firmware to allow programmable BUSY 'level'**
3	**10bit FADC250**	**DAQ Lab** **SN003 Moller** **SN007 Moller** **SN001 Spare**	**Received from ORNL**
1	**10bit FADC250**	**DAQ Lab** **SN005**	**Needs repair;** **Clock Issues**
1	**12bit FADC250**	**EEL109**	**Returned to Jlab for firmware check**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Programmable Token passing scheme works. Enable register has been added.** **BUSY signals are OR'ed and enable register works.** **FADCTrigOut signals are OR'ed and have an enable register**

0. Trigger/Clock/Sync – TI/TD

19 June 2009

Please see the Firmware section for updates.

12 June 2009

Several iterations of Altera firmware have produced a working Token passing and control scheme. Abhishek has firmware that implements an enable register for each payload port, and the token passing scheme was measured with four (4) FADC in the VXS crate with the Wiener backplane. The payload port map enable firmware was mapped for the Elma 20 slot backplane, but after writing the correct port enable pins, the boards were read out with 2eVME and token passing. FADC were in PP16, PP12, PP10 and PP14.

Trigger Rate: 100 KHz

128 Block Events: TI setting

30MB/s data transfer rate. (6 input signals distributed to 4 FADC modules)

29 May 2009

Token passing implementation is the next (and final) test for the suite of prototype modules. There was a discussion about the TI and it was stated that the TI must be the first module (source) in the token passing scheme. (Dave Abbott) Presently the TI does not have a token passing signal to the SD and we will need to assign single ended pins on the P0 connector for BUSY, and FadcTRIG_Out so that the Token In and Token Out can use the differential signaling.

1. FIRMWARE TESTING

19 June 2009

→Ed reports that the BUSY level assertion register has been added and that it functions correctly. This will allow programming of the FADC250 so that a BUSY signal will be generated at increments smaller than the full front end buffer time.

→Maximum trigger rate testing.

The discussion started with Ed explaining a few issues with the 2eSST software patch that is a 'work-around' a few issues with the Tundra 2eSST chip and large blocks of data. There are several combinations of backplane readout modes with and without token passing that have been accomplished so far. For example, the data results for the IEEE-RT conference poster was transferred with 2eSST but without token passing through the SD. (Please send updates)

To achieve the highest trigger rate we will have to implement 2eSST, with token passing through the SD, and with the BUSY signals OR'ed through the SD to provide feedback to the Trigger Interface. To achieve the maximum trigger rate and not saturate the VME readout bandwidth, the FADC250 modules will need to be in 'pulse' mode. The maximum trigger rate and data rate testing has not been completed yet, but it sounds like all the hardware and firmware is in place. Ben has been very busy with a few other projects, but hopefully we can set this up before the trigger workshop.

12 June 2009

→Ed reported at the 5 June meeting that he will implement a register to program a BUSY assertion 'pointer'. (My definition for lack of a better term) Presently the BUSY from each FADC will almost never be asserted because the buffer size is large. For testing the BUSY it will be necessary to be able to set the point at which the BUSY is asserted.

→There has been other firmware work but it is primarily associated with the Hall A Moller application and I have placed the information under the 'customer' section.

29 May 2009

Hai's new LX25 firmware will be loaded on at least three FADC250 and tested at the highest trigger rate possible. Ed has completed the token passing firmware and this has been tested using the 2eSST transfer mode. The token passing scheme presently uses P2 wire jumpers to connect the FADC250 modules in the crate.

Abhishek is working on the firmware to control the selection mask registers for the token passing, BUSY signals, and trigger_Out signals. The clock selection register will also need to be tested. Users can select from three clock signals for each half of the crate. (Odd and Even Payload modules)

The Altera interface needs to be changed to interface the new requirements for the Moller application. Ed will need to alter this firmware.

2. *SUB-SYSTEM PROCESSOR (SSP)*

19 June 2009

Ben showed the progress of the SSP schematics at our Electronics Group meeting and it is impressive and the Altium tools will be put to the test for the management of the FPGA netlist. It is not clear that the Altium tools provide a seamless connection to the Xilinx design tools, especially since we are using a Xilinx library part (V5LX110) that is pin compatible with the V5FX70 that will be used on the board. One step at a time, and so far the Altium tool shows some very nice features for managing pin/gate swapping, hierarchy functions, and enhancements to the board layout methods especially for replication of sub-circuit sections.

12 June 2009

No report, but Ben has started with this design process and has figured a way to use the FPGA tools in Altium to connect the necessary signals for the Gigabit Transceivers and other important nets to what is defined as the "manual" page in the FPGA schematic design tool. The SSP is schedule for FY10, and takes 2nd priority to the 16 channel discriminator project.

29 May 2009

Ben has corrected Chris' hierarchy errors, and has started to work on the design. There is a significant amount of work to accomplish on the schematic, but virtually all of the integrated circuits have been selected for the design.

3. CUSTOMERS

19 June 2009

→The firmware for the Hall A Moller system is complete and tests are progressing in the Daq Lab. Two FADC250 boards will be allocated for this experiment period; one board is a spare.

→Ben reports that the 12 bit FADC250 board has been received from the IU FCAL group. Apparently there is something wrong with a channel on the board. The last thing that was changed was an 'upgrade' to the latest firmware revision. Hai mentioned that he suspects the problem might be a timing issue between the 12 bit Maxim parts and the 10 bit Maxim parts. It is not clear how soon the IU FCAL folks need the 12 bit board returned, but it will take a few weeks to understand the problem and provide a fix.

→Chris mentioned that Paul Eugenio was seeking to use a FADC250 module and it is not clear if the IU FCAL group was willing to let Paul use it for his TOF testing. It is probably a long shot, but worth talking to both groups to see if something can be worked out. Paul has another issue with a non-VXS crate, so the 12bit FADC250 would work fine because the J0 connector is not populated.

12 June 2009

Hai reports that Ed is finished with the firmware for the Altera FPGA and is testing the new firmware with the new firmware implemented on the FX20 for the Hall A Moller experiment. There was a recent meeting with Brad S. from Hall A to discuss implementation details, and two FADC will be allocated for the duration of the Moller experiment. The experiment begins 21 August, so there is time to verify the new firmware, and install the module in its final configuration in the Hall, and test in the Hall before beam delivery.

29 May 2009

Hai has completed the firmware development and simulation verification for the Moller experiment requirements. There are a few firmware functions that Ed will need to complete to control registers in the 'FX20 that are different from the other FADC250 modules. Two FADC250 modules will be 'reserved' and tested for the Moller experiment that is scheduled for Aug09.

Testing in the lab using the pulser fanout module will be useful to verify the operation of the new firmware features for the Moller application. Presumably there will be modifications required for the CODA library for use in the Hall, and we can get a status update from Dave A. at the next meeting.

4 "B" Switch - Signal Distribution Module (SD)

19 June 2009

Abhishek reported that the final changes to the control register firmware have been tested. The Token In/Out signals can be enabled via a register and this prevents signals from passing to empty payload slots. The Token bypass testing was performed in the Wiener 21 slot VXS crate, and the 'special' payload port mapping is handled by programming the SD to bypass the required slots. The BUSY signals from each payload port are managed in the same fashion and this was also tested.

The SD document needed significant updates and the final draft is in circulation for edits. There will be a few modifications to the next revision, and Mark will handle the transfer of the SD PCAD design to Altium. The initial steps will be to include all ECOs and gather any new requirements for the SD features as we progress with other trigger modules.

12 June 2009

→Ben has included the SD module in the test stand configuration GUI and is able to program the SD modules to bypass the empty slots. The SD firmware appears to work properly and transfers the token passing signal to the FADC that are configured in the VXS crate. The 2eSST mode was not attempted (I do not recall what the reason was) but this mode will be verified soon. The BUSY and FADC_TrigOut signals have programmable mask registers and presently both of these signals are simply OR'ed in the SD Altera FPGA. The BUSY signal is transferred to the TI and SD front panel, and the FADC_TrigOut signal is driven only to the SD front panel.

→After some discussion, Ben suggests that it would be a nice feature to use the FADC_TrigOut signal in a way that the SD board could automatically configure during initialization. The CTP could also use this method too, except the CTP would have to use some special message from each FADC's serial stream during the initialization process. The TI could verify that both CTP and SD report that the same PayloadPorts are functional, and set the PayloadPort mask register to the SD and CTP. More details and explanation at the Trigger meeting.

29 May 2009

Abhishek presented his latest work on the firmware and testing of the SD module. Work is progressing, and the output signals were shown to be 'registered' with the on board 50MHz clock. The outputs for the BUSY, Trigger_Out and Token passing signals should not be registered and this will be changed in his firmware and verified in the lab.

One SD board will need to be fully tested in the VXS crate with at least four FADC250 modules. Ben will need to include the register control features to his test stand code(GUI) for the SD and verify that clocks can be programmed for each side of the crate, plus test that the SD programmable features for masking empty payload slots for the TOKEN and BUSY signals work properly.

I have asked Mark to begin the process of transferring the final SD prototype files from PCAD to Altium. Mark and Abhishek have kept a record of all the ECOs required for the final version and these ECO will need to be included on the Altium schematic. There are a few decisions to make regarding the pin assignments for the BUSY, TOKEN, and TRIG_OUT signals, and these will be included on the Altium schematic.

5. System Diagrams & Test Stand Activities

June 19 2009

Nothing new to report on system diagrams, but this is the best spot to list the discussion on the price estimates from Wiener on their 21 slot VXS backplanes. It is clear that they want us to use their "Hartman" payload port map. Hartman will design a 21 slot VXS backplane with the ELMA payload port map, but it will include significant cost for the NRE. It is clear that we want to use the ELMA map because there are several vendors that have these VXS backplanes as stock items. The Harman backplane design includes a VME64x slot which is a nice feature but not a requirement. It was mentioned that another option would be to approach CAEN because their VME card enclosures and power supplies are almost identical to the Wiener. CAEN would have to provide a VXS 20 slot ELMA mapped backplane, but that is up to them to meet the specification.

June 12 2009

The IEEE-NPSS Real-Time conference papers have been uploaded and accepted. If you would like to browse the presentations please visit:
http://indico.ihep.ac.cn/conferenceTimeTable.py?confId=456

29 May 09

→No report on the new LabView test code operation. Mark has been very busy with other projects, but the application code is ready for a test with the new controller and LabView code version.

→The poster and talk at the IEEE-NPSS Real Time Conference went well and we had a unique solution using VXS. It was great to see the development with ATCA for Physics, and virtually every presentation showed some type of high end Xilinx or Altera FPGA processing front end data and extensive use of fiber optics to drive the data from the front end circuits. From my notes, we seemed to be the only group using the 12 fiber connectors, and other folks were interested in this technology. The MTP connectors and multiple fiber link certainly makes the fiber connections much more manageable.

It was interesting to hear about the upgrade to LHC already, and plans for 'triggerless' systems. I thought the technology planned for the ITER reactor is fascinating and for $10 Billion Euro one has many choices.

→What other testing to complete in the Trigger Test Stand?

- Need to verify operation of all SD programmable features with multiple FADC250 boards
- Use new firmware and test to >200KHz trigger rate
- Measure data transfer rate at highest trigger rate with 2eSST
- Include token passing with 2eSST
- Verify Moller application code

6. Crate Trigger Processor (CTP)

19 June 2009

CTP is ready for the maximum trigger rate testing!

12 June 2009

Hai reports that the CTP is ready for use with one crate, four board testing plan. We will set this up using the programmable SD, with token passing, and 2eSST and record the maximum trigger rate. BUSY will need to be working and sent to the TI so that the system is stable during the test.

29 May 09: No report

ACTION ITEMS: **Next meeting will be at CNU for the Trigger Workshop!!**

2nd Annual Trigger Meeting scheduled for 8 July 2009 @CNU
Please register at:
http://www.jlab.org/Hall-D/meetings/online_workshop2009/Registration/Register.php