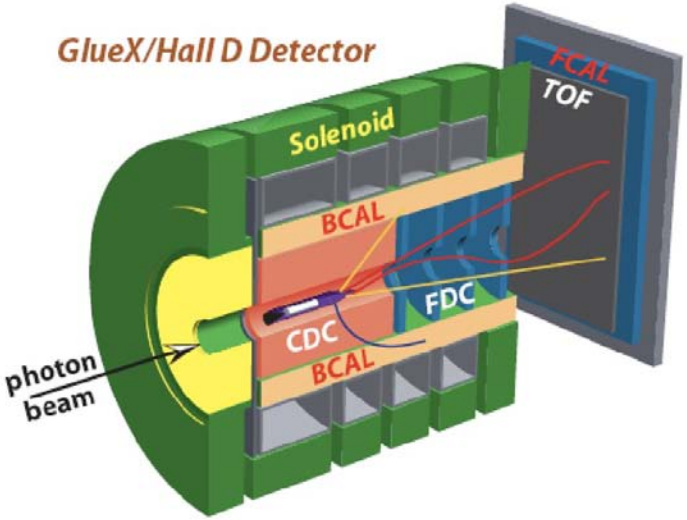
A 250 MHz Level 1 Trigger and Distribution System for the GlueX Experiment



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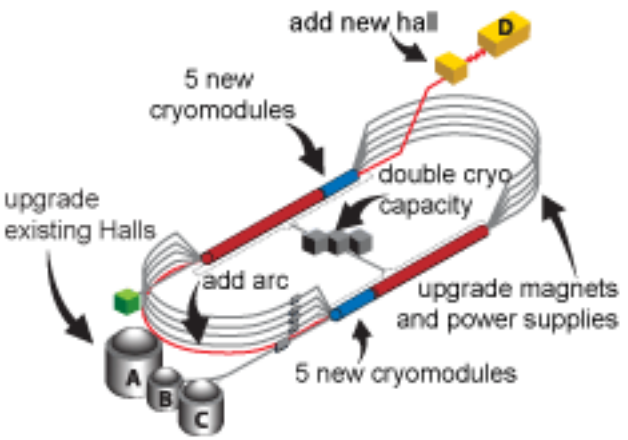
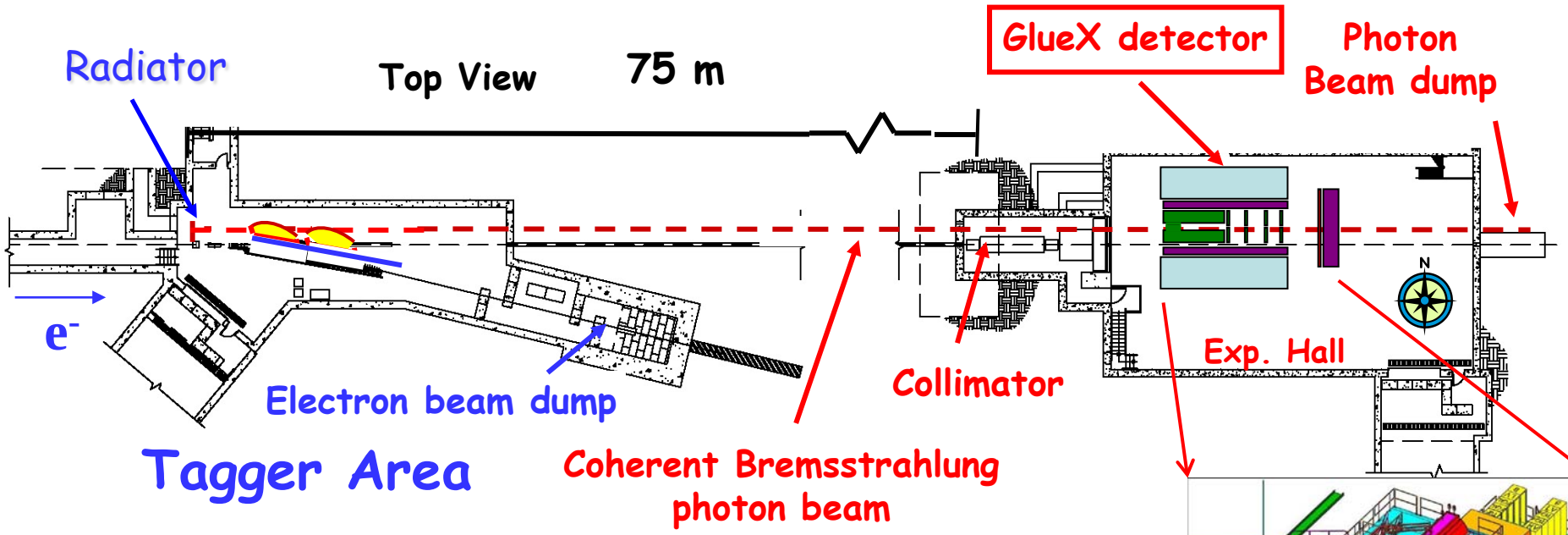
Introduction

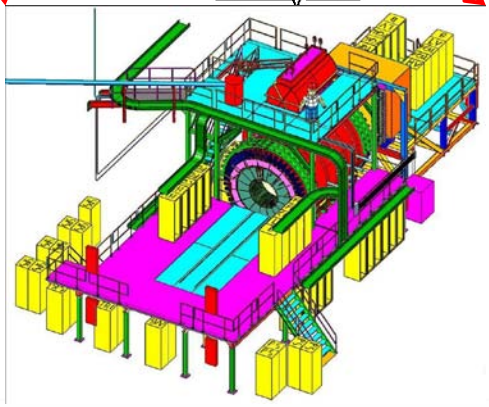
- Jefferson Lab (in Newport News Virginia) has begun construction on an upgrade to the existing electron accelerator.
  - Double the energy – 6 GeV -> 12 GeV
  - Fourth experimental area (Hall D)
  - Completion by 2015
- The new experimental Hall will house the GlueX detector
- New experimental program will require upgrades to existing DAQ and trigger systems. All experimental halls share a common DAQ system (CODA).
- New designs are being introduced into the existing 6 GeV program.



GlueX Experiment

Physics goal: Search for exotic mesons in interactions of polarized photons with a hydrogen target





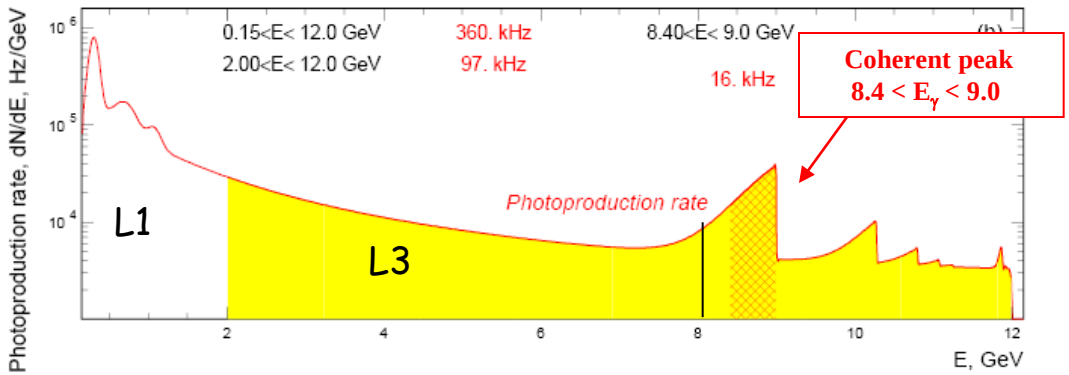
- Bremsstrahlung photons produced by 12 GeV electron beam incident on a diamond crystal. Main coherent Bremsstrahlung peak at E_γ 8.4 – 9.0 GeV
- Two classes of interactions in the detector:
  - Hadronic photoproduction (on 30 cm long liquid hydrogen target)
  - Electromagnetic interactions

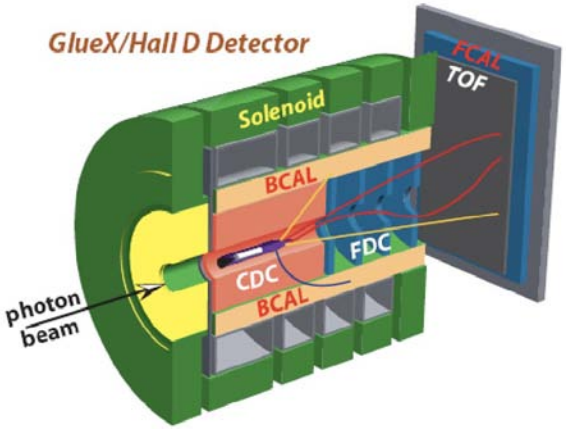
GlueX Trigger

Total Photon flux : 3 x10^9 (10^8 in coherent peak)
Total Hadronic Rate: 360 kHz
Total Elecromagnetic background: ~200 MHz
(Compton + pair production in target/detector)

Trigger: **Level 1** (Hardware) + **Level 3** (Software)

L1 Goal: < 200 kHz
(with high efficiency for coherent photoproduction)





Total Channels: ~22k
L1 Data rate: ~3 GB/sec
L3 Farm: 20 kHz, 300 MB/s to Disk
Detector subsystems:

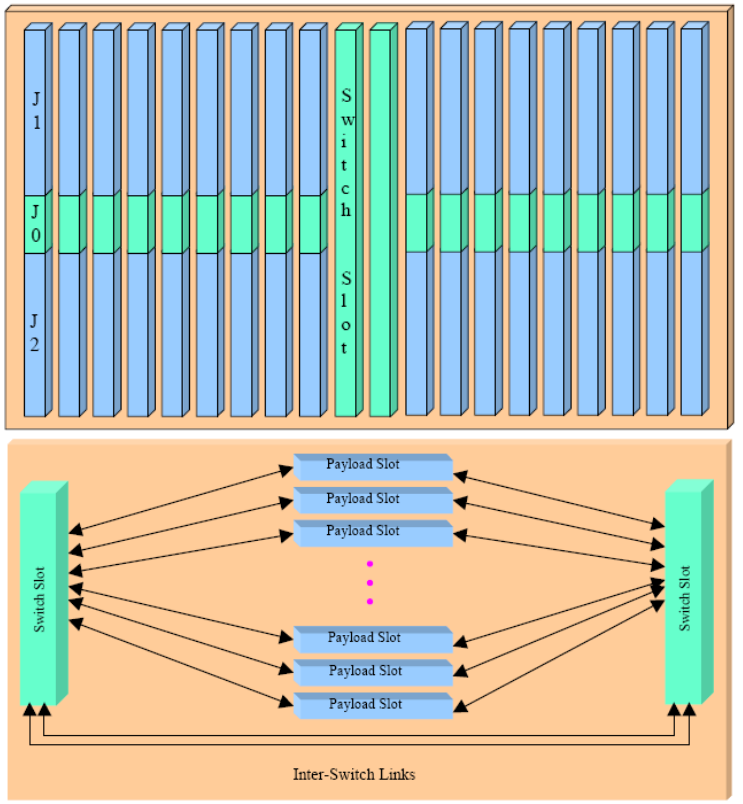
- Tagger (L1)
- Pair spectrometer
- Start Counter (L1)
- Central Drift Chamber
- Forward Drift Chambers
- Time of Flight (L1)
- Barrel Calorimeter (L1)
- Forward Calorimeter (L1)

Level 1 Design

- Up to 5 detector subsystems can be used
  - FCAL/BCAL – Energy
  - Start Counter – Hits
  - Forward TOF – Hits
  - Tagger – Hits (not at high luminosity)
- Continuous computation (@ 250 MHz)
- 4 level hierarchy

  Board -> Crate -> Subsystem -> Global
- VME for the Data Path (2eSST : >200 MB/s)
- VXS for the Trigger Path
  - 18 payload slots
  - 2 switch slots (redundant star)
  - 8 serial lanes (4 each in/out) per VME slot

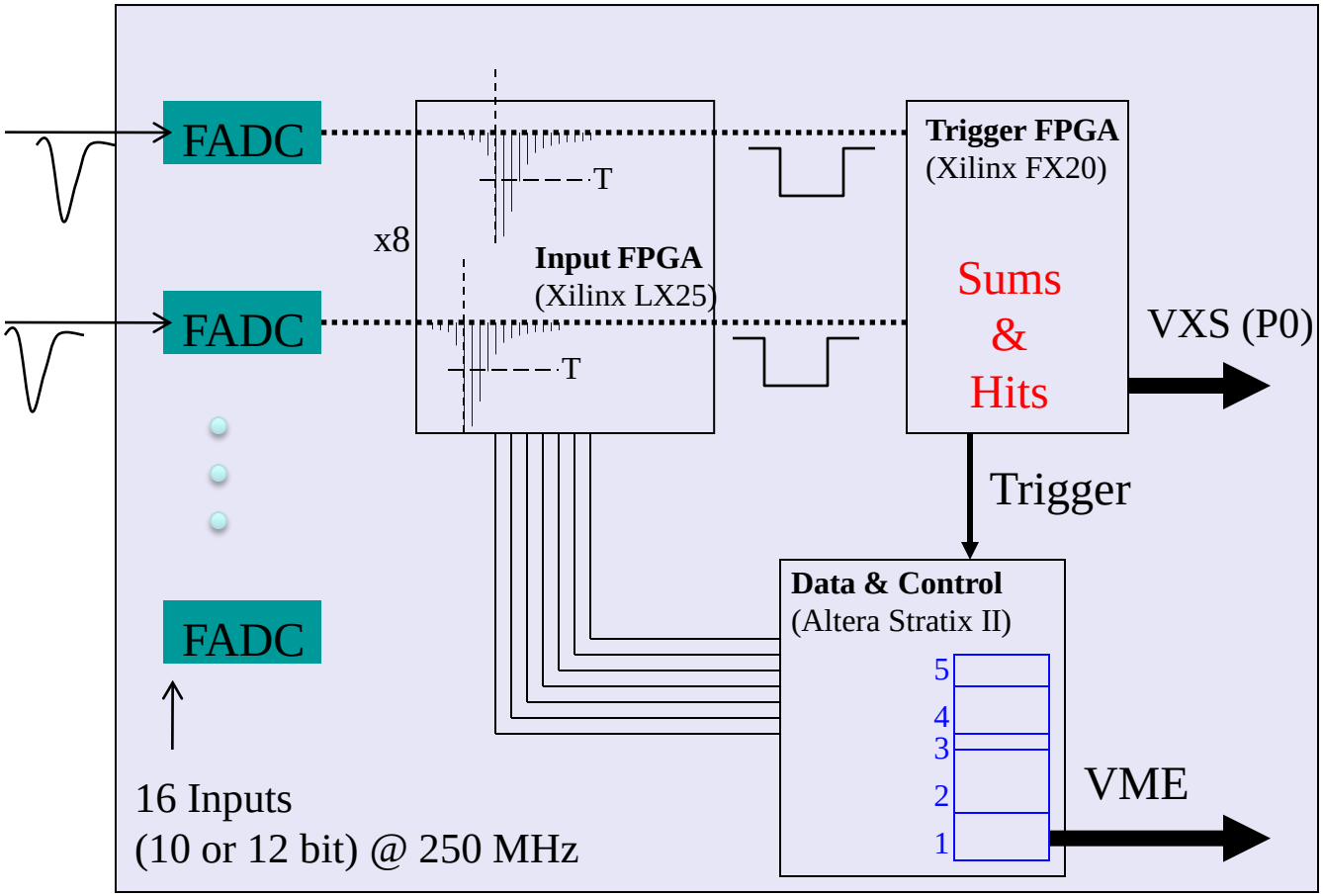
- Board level trigger starts with custom JLAB design flash ADC (250 MHz)…



VXS (VITA 41 standard)
VME64x + high speed
serial fabric on J0

JLAB 250 MHz Flash ADC

- Pipeline trigger/data (8 microsec lookback)
- User downloadable (via VME) code for Input/Trigger FPGAs



Rocket I/O
Aurora protocol
x2 lanes bonded
2.5 Gbps/lane
8/10 bit encoding
Data: 500 MB/s

2eSST
Data: 200 MB/s

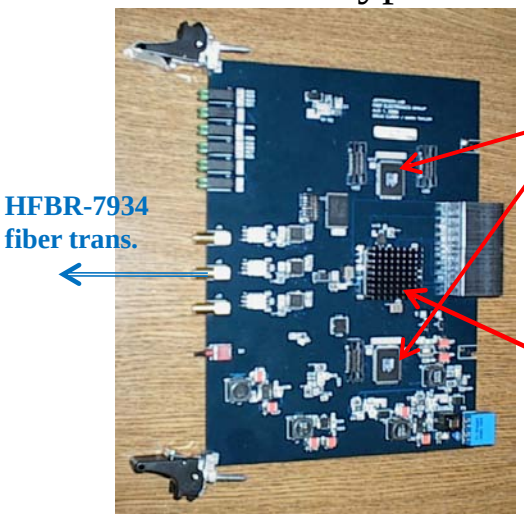
Crate Level Processing

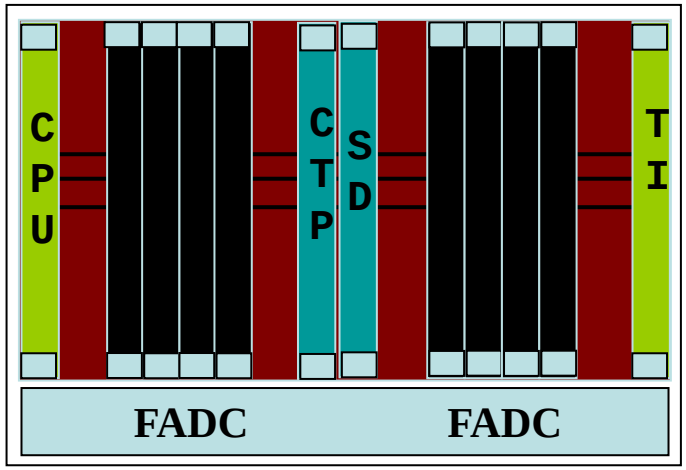
- Crate Trigger Processor (CTP)
  - Switch slot A
  - Accept 16 FADC streams via VXS
  - Crate Sum & Hit processing
  - x4 lane (1 GB/s total) fiber out to sub-system level

- Trigger Interface (TI)
  - Payload slot 18
  - Accepts Global Trigger/Clock/Sync Info
  - Fixed Latency link (16 bits @ 62.5 MHz)
  - Sends trig data to SD for crate distribution
  - Accepts CTP info for VME readout

- Signal Distribution Card (SD)
  - Switch slot B
  - Distribute (via VXS) Clocks/Trigger/Sync to all boards in the crate.

CTP Prototype

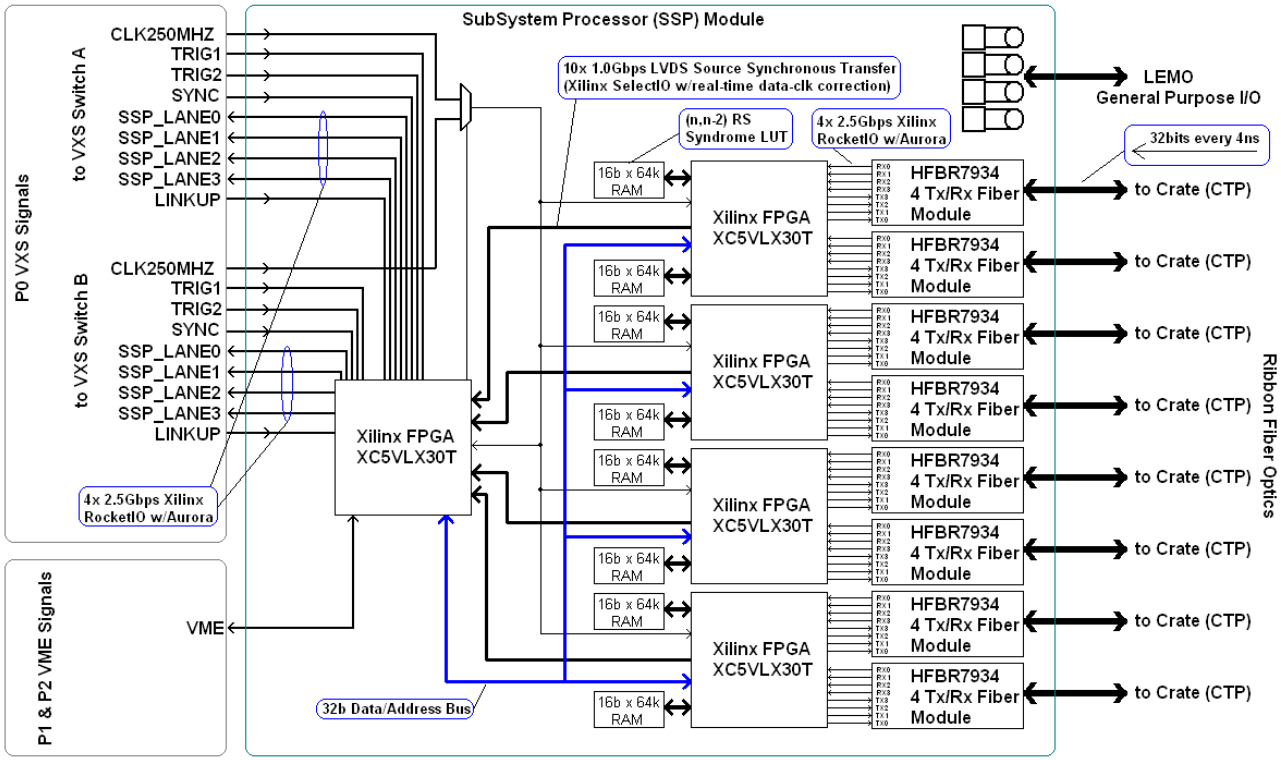




VXS Crate

Sub-System Processor (SSP)

- All SSPs reside in a single VXS crate (Global Trigger Crate)
- Each SSP receives up to 8 four-lane CTP links
- Multiple SSPs will be needed for some Detector systems
- Each SSP clock time-stamped reports to Global Trigger Processor (via x4 lane VXS)
- Prototype designs are in progress



GlueX L1 Systems:

```
BCAL: 2 SSPs
FCAL: 2 SSPs
SC  : 1 SSP
TOF : 1 SSP
TAG : 1 SSP
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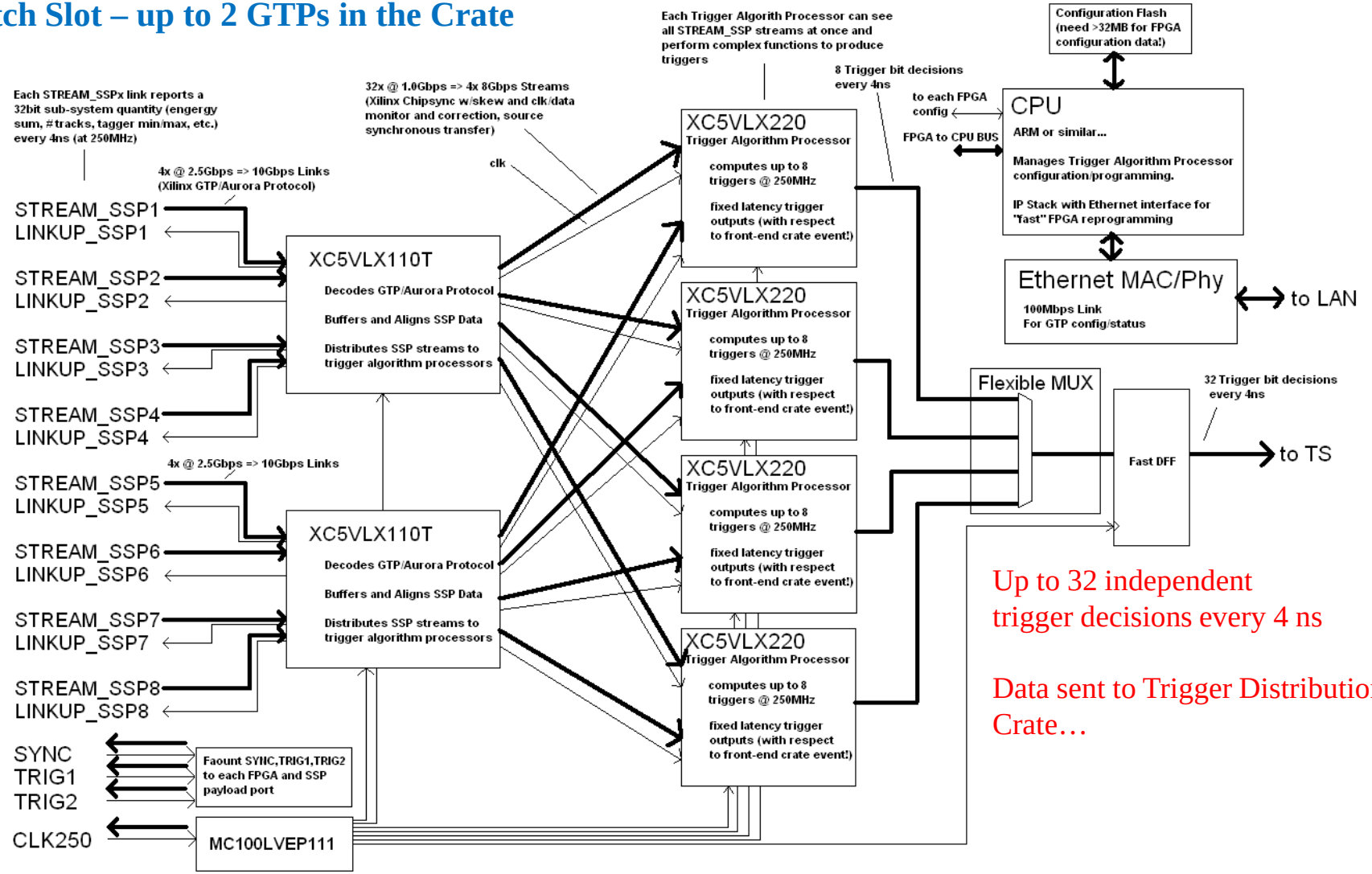
Global Trigger Processor (GTP)

Switch Slot – up to 2 GTPs in the Crate



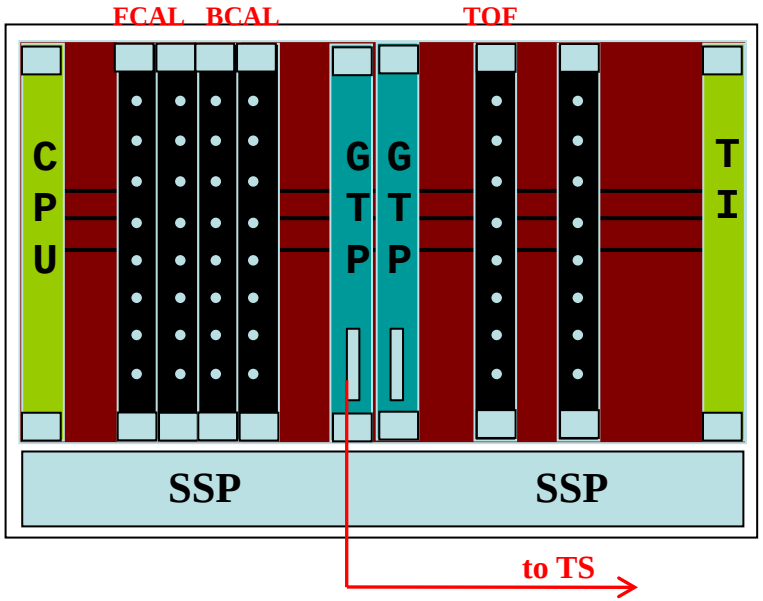
Up to 32 independent trigger decisions every 4 ns

Data sent to Trigger Distribution Crate…

Global Trigger Processing cont…

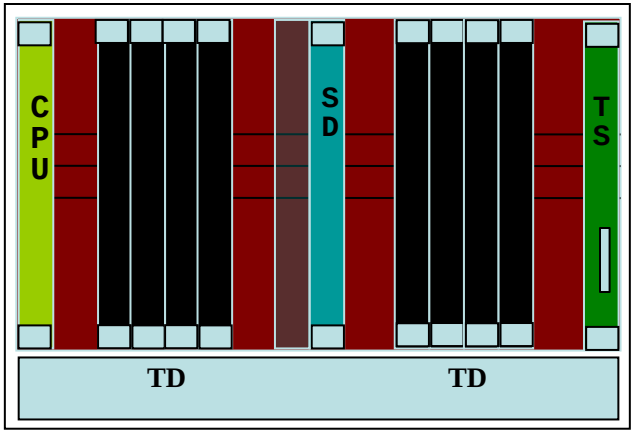
To estimate the latency involved in calculation of an L1 trigger by the GTP an example equation was implemented in VHDL using Xilinx synthesis tools and a Virtex 5 LX220 FPGA:

Z >= TFM*HTOF + EFM*EFCal + RM*((EFCal +1)/(EBCal + 1))
HTOF - Hits Forward TOF
EFCal - Energy Forward Calorimeter
EBCal - Energy Barrel Calorimeter



- All computing done in pipelined, 32bit floating point arithmetic
- SSP data was converted from integers to floating point
- Equation is computed every 4ns and trigger bit is updated if Z is above a programmable threshold
- Each coefficient is “variable” – can be changed very quickly without having to reprogram FPGA
- Used Xilinx specific math libraries (+, -, *, /, sqrt)
- Synthesis and implementation resulted in using only 3% of LX220 FPGA
- **Latency was 69 clock cycles => 276ns delay introduced for forming L1 trigger**

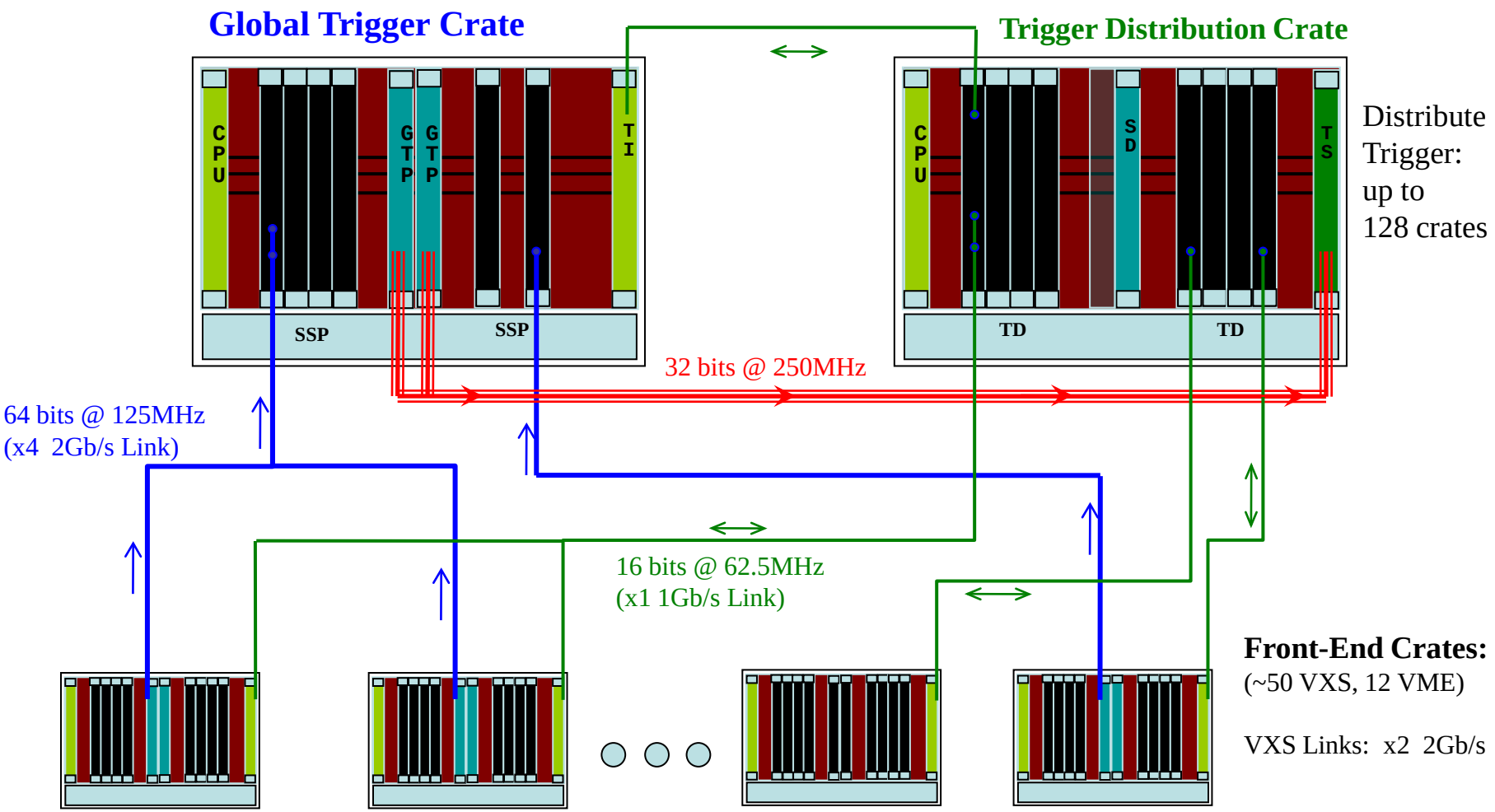
Trigger Distribution



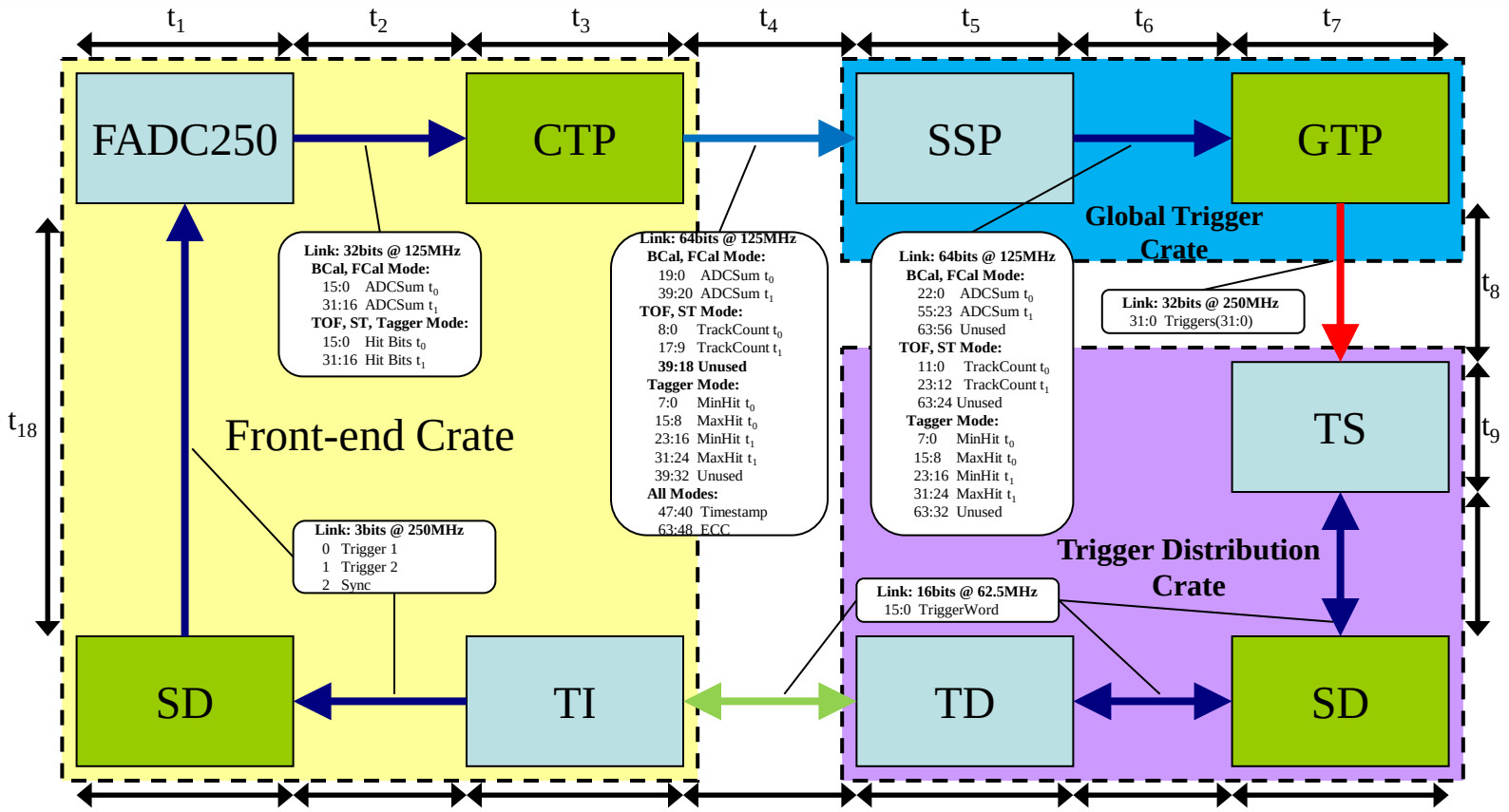
- **Trigger Supervisor (TS)**
  - Accept trigger decision from GTP (ribbon/copper)
  - Async User triggers – pulsers/calibration
  - Source for global 250 MHz Clock
  - Serialize trigger :16bits @ 62.5 MHz (every 16 ns)
  - "Master" TI board – payload slot 18

- **Trigger Distribution Cards (TD)**
  - up to 16 total (in payload slots 2-17)
  - Fan-out clock/trigger/sync to 1-8 crates (to TI)
  - Uses same fiber connections as CTP->SSP links
  - Ensure fixed-latency link for trigger to all front-end crates
  - Synchronizes 250 MHz clock on all crates
  - Return data link provides crate status – error or busy condition that would require triggers to be disabled.

L1 Trigger & Distribution

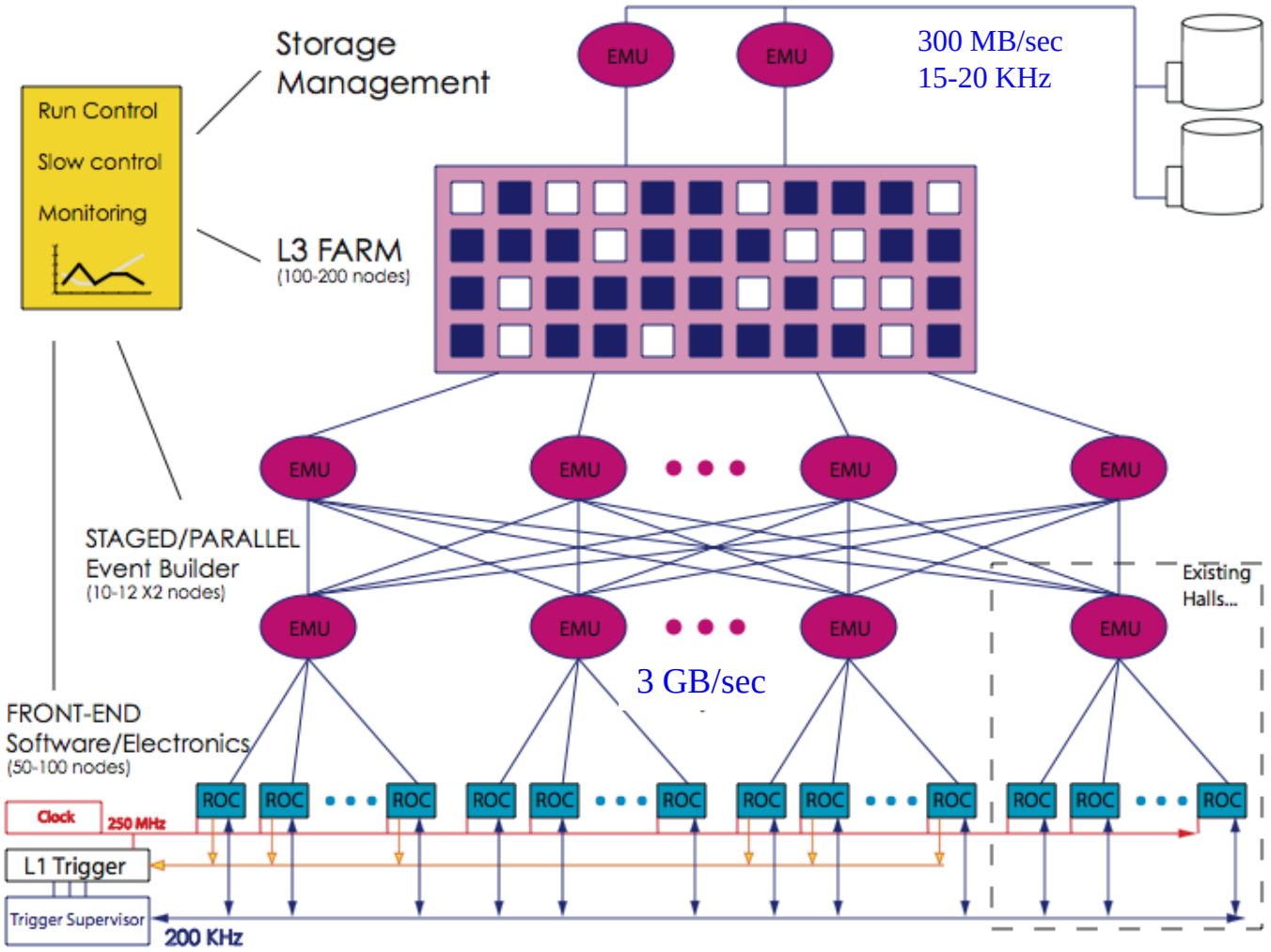


Level 1 Trigger Timing



t_1: FADC250 (ADC->P0)	180ns (20cycles+100ns MGT)		t_{11}: SD (Px->Px)	10ns	
t_2: FADC250->CTP (P0->Px)	10ns		t_{12}: SD->TD (Px->P0)	10ns	
t_3: CTP (Px->FiberTx)	180ns (20cycles+100ns GTP)		t_{13}: TD (P0->FiberTx)	10ns	
t_4: CTP FiberTx->SSP FiberRx	600ns (~100m fiber run)		t_{14}: TD->TI (FiberTx->Fiber Rx)	600ns (~100m fiber run)	
t_5: SSP (FiberRx->P0)	600ns (100cycles+200ns GTP)	t_{15}: TI (FiberRx->P0)		80ns (20cycles)	
t_6: SSP->GTP (P0->Px)	10ns		t_{16}: TI->SD (P0->Px)	10ns	
t_7: GTP (Px->TrigBit)	495ns (95cycles+100ns GTP)		t_{17}: SD (Px->Px)	40ns	
t_8: GTP->TS (TrigBit->TrigBitIn)	10ns		t_{18}: SD->FADC250 (Px->P0)	10ns	
t_9: TS (TriggerBitIn->P0)	115ns (20cycles+35ns SerDes)				
t_{10}: TS->SD (P0->Px)	10ns		**Total:**	**2980ns**	

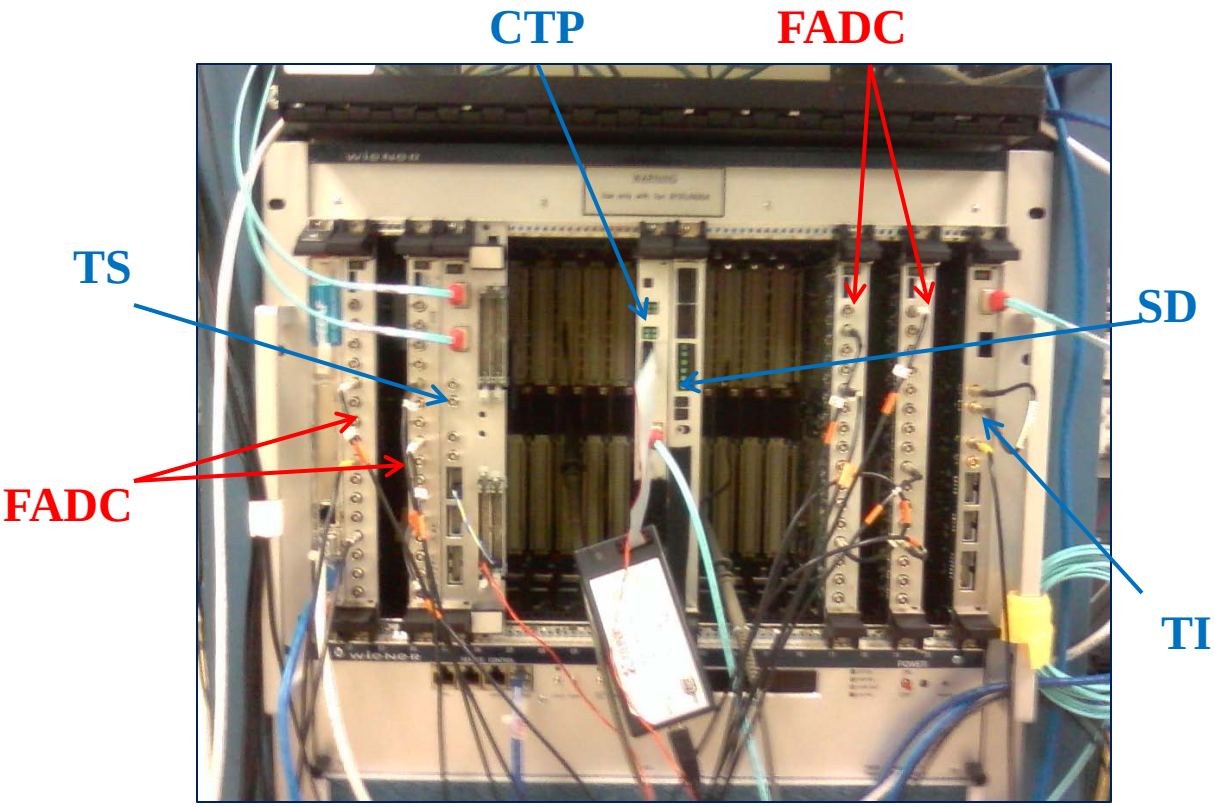
GlueX DAQ Overview

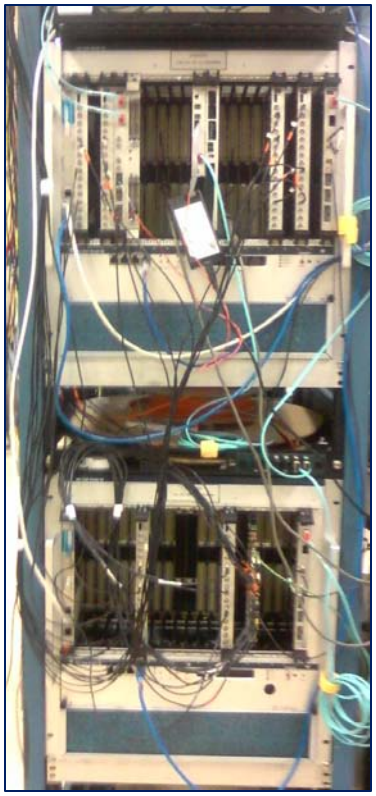


Prototypes & Testing

- Two crate system
- Crate-level summing (4 Flash ADCs)
- 250 MHz clock distribution
- Trigger distribution/ synchronization (up to 150 meters)

Please visit Poster
TDAP-16
for more information





Summary

- The 12 GeV upgrade and a new experiment (GlueX) at Jefferson Lab requires significant performance improvements for both trigger and data acquisition.
- We must transition with support for legacy systems in the other experimental halls - VXS.
- Implement deadtimeless pipelined front-end digitizers with synchronous 250 MHz Level 1 trigger and distribution system.
- L1 requirements (200 kHz, < 4 μs) latency can be met.
- Customized L1 systems can be built from for all experiments using

  Board -> Crate -> Sub-system -> Global hierarchy
- Prototyping and testing have been successful without pushing the bandwidth limits of the technology. There is much room for expansion.