

## **12GeV Trigger meeting notes:**

13-April-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, B. Moffit, H. Dong, J. Wilson, E. Jastrzembski

30-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson, E. Jastrzembski

23-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson, E. Jastrzembski, Beni Z.

16-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, B. Raydo, S. Kaneta, B. Moffit, H. Dong, J. Wilson

9-March-2012: C. Cuevas, W. Gu., A. Somov, N. Nganga, S. Kaneta, B. Moffit, H. Dong, E. Jastrzembski

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### **0. Trigger/Clock/Sync – TI/TD**

#### **13April2012**

TID technical evaluation team is finished and the final award is delayed for a short time because the companies will have to provide best and final cost proposals based on lower quantities. (Hall A cannot fund 9 units this FY)

Functional test with the rear transition board is positive and still needs to be tested with the GTP.

#### **30-March-2012**

Rear transition board assembled and William has a finished board for show.

TID procurement is at the best and final stage, with a few technical questions to the vendors and hopefully a reduction in price.

TS is a final draft and will evolve.

#### **23-March-2012**

Vendor source evaluations are due to William for the TID production units. By next Monday the summary report will be sent to Kathleen.

TS manual in progress and no other test results presented. Rear transition board has been assembled and will be tested with the GTP soon.

#### **16-March-2012**

4 proposals have been received with the final evaluations due next week by the tech review committee.

→TS initial testing:

Rear transition board is not assembled yet, but will be soon so testing with the GTP can begin soon. Firmware and new TS library development is in progress.

#### **9 –Mar 2012**

Bid schedule on track. Will need to evaluate proposals within 5 days.

TS prototype (1<sup>st</sup> article) is in the initial test stage, with plenty of firmware development in progress. BUSY circuits are being tested.

The global trigger consolidated crate idea will work and needs to be discussed with the Hall A and Hall C DAQ folks.

PEPPo solution with the pipeline TI is solved. (Interrupt issue with TI) New firmware application for PEPPo (helicity integration mode) is ready for testing.

## 1. SUB-SYSTEM PROCESSOR (SSP)

### 13April2012

SSP firmware and GUI for the HPS displays has been developed. Final testing with the new firmware changes to CTP and FADC250 for the HPS test run is in progress. (EEL109)

uMegas detector group has requested firmware and schematics for the SSP. They are planning to use the SSP in a slightly different mode to read out their detector channels. Formal note needed to send the firmware to the uMegas group.

### 23-March-2012

Ben has requested changes to the CTP-FADC250 code. No show stoppers seen, but lots of work to complete before installation and use on the HPS experiment.

Production SSP work has not been started, but minor ECO and any other changes will need to be completed before production order is placed.

### 16 March 2012

Simulated CTP input data streams to reflect the HPS setup. More testing will be needed before installing in the hall.

## 2. CUSTOMERS

### 13April2012

PEPPo folks are happy for now, but seem to have a few pesky noise issues that they would like to apply a firmware solution.

Hall D tests are going well. BCAL test is set up in the hall!

HPS setup is going well in the EEL109 and will be moved to the hall next week. Hall is open on Thursday 12-April for installation and initial testing.

### 23-March-2012

→PEPPo FADC250 board has been repaired and is ready for final test. Deliver by 26-March.

→HPS

- At least 9 more FADC250 modules have been located and will need to be tested. There are still issues with the units that have been tested, and so far none of the boards pass the test 100%.

→Hall D – FCAL beam testing (ongoing)

→Hall D – BCAL beam testing (proposed for April)

→Hall D – Pair Spectrometer will use several FADC250 boards

### 16 March 2012

→Test and repair activities are progressing with the FADC250 that are not functioning at 100%. There are several issues and these modules do not pass the low level functional testing step.

Discussion to purchase Ethernet to JTAG interface so that any firmware downloads to the CTP can be performed remotely. Hall B funds will plan to purchase these items.

→PEPPo firmware development work is nearly complete and has been a significant effort! The future positron machine is close to reality!

→Customers are abundant!

-Hall B -- HPS beam test (March -> May)

-Injector – FADC250 firmware modifications

### **3. “B” Switch - Signal Distribution Module (SD)**

#### **13April2012**

Final Technical Evaluation Team has completed the scores on the bids and the prices were under the estimate. There is a late twist in the ordering plot because Hall A apparently does not have the funding allocation for 9 boards.

New procedure for acceptance testing the SD production boards has been drafted. The idea is to use 16 fully tested FADC250 boards to verify the individual SD production boards.

Front panel has been ordered for the SD. Looks like we will have 9 extra front panels IF nobody picks up the extra nine boards.

#### **30 March 2012**

→Vendor prices were revealed and we will request another week to evaluate best and final offers. Four of five vendors were acceptable, and hopefully the overall prices are reduced after best and final offers are delivered.

#### **23-March-2012**

→SD production board fabrication and assembly bids have been evaluated and summary sent to procurement. The prices for the production quantities have been revealed to the source selection committee. No final decision yet, but the award will be ratified soon.

→Acceptance test plan discussion was very useful and insightful. In the end, we will plan on using 16 of the production FADC250 modules to fully verify the proper operation of each production SD module. Using 16 fully tested FADC250 boards in the SD acceptance test procedure will eliminate the need for the test operator to cycle the crate power and change the location of the payload test board. Great discussion and Nick will have to modify his existing test procedure.

#### **16 March 2012**

Five proposals received with one not truly acceptable. Evaluation summary will be submitted to procurement next week.

→HPS installation and test will take higher priority than the SD acceptance test procedure.

→As soon as the procedure is at a final draft, one of the technicians should perform the procedure from scratch.

#### **9 March 2012**

Proposals are due today, with 5 days of evaluation.

Acceptance test procedures in place and ready for production boards. 10 1<sup>st</sup> article boards.

Initial test procedure will be executed in EEL109 next week by one of the techs to see if the procedure is reasonable or requires modifications. Front panel PRs are complete.

#### 4. System Diagrams/Fiber Optics

##### 13 April 2012

No report.

##### 16 March 2012

Brad S. (Hall C) suggested a simple MTP Fiber test in hall c using a few of the short jumper cables. The suggestion is to simply place a fiber patch cable in Hall C for the remainder of the 6GeV experiment and then test the fiber cable to see if there is any transmission problem. Setting up an 'active' test would take some effort with hardware/software using an evaluation board and the 150m fiber. This way a measurement of fiber degradation over a finite time interval with a known dose rate could be achieved. Ben, Chris, Brad.

#### **5. Two Crate DAq test configuration**

##### 13April2012

No huge issue, but one item in discussion is that the 2<sup>nd</sup> CTP appears to have an issue with the CTP output fiber transceiver. Apparently the timing constraint is marginal, and when Scott returns there will be fine tuning to complete. SSP and GUI work progress is going well.

There may be some firmware change to compensate for the offset contribution to the trigger 'data' sum that is sent to the CTP. At the Wed Hall B meeting, we decided to move forward with the existing firmware and establish a procedure to measure the offset (synonymous with pedestal)

##### 30 –March-2012

HPS hardware testing is prepared in EEL109. Need fibers for CTP to SSP, but everything else should be ready to test.

Plan is to move the hardware to the Hall B CH by end of next week 6-April-2012!!

Then, the boards will be moved to the Hall.

##### 23-March-2012

Same report as last week and a few discussions regarding the details of the procedure have been exchanged. (Bryan – Chris) There has been discussion about setting up multiple locations to test full DAq crates, and there will be several types of full DAq crates tests to develop.

##### 16 March 2011

→Some discussion about the full crate testing and presently we do not have enough modules to proceed with this effort. We will need to have a draft procedure soon, and will also need a 'standard' CPU setup for the full crate tests.

##### 9 March 2012

Legal and illegal register ranges, etc. New library developments for latest trigger modules in progress.

##### 20-JAN-2012 (Keep this date reference full DAq crate procedure)

##### 3 June 2011

**→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!**

16 July 2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

#### 6. Crate Trigger Processor (CTP)

### **13April2012**

Annotation problems have been resolved. Schematics and PCB are verified to match and the schematic changes (ECO) will be started next week. PP17 will be wired to the FPGA so that if we wanted to use the Gigabit protocol from the ROC it could be attempted. MUST keep this a high priority to meet the production schedule for Hall D.

After the HPS test run, we will need to evaluate the CLAS12 design requirements for the CTP. Their needs will probably require a higher performance chip or chips. Hai will evaluate the cost to increase the VirtexV chips on the Hall D production boards to the fastest grade and highest performance. (Logic gates)

### **30-March-2012**

CTP CAD issue has been resolved, (Thanks Scott) Keep this on track for Hall D production order by summer!!

### **23-March-2012**

→Need to revisit the schedule for the production CTP activity. There are still a few problems with the transfer of the CAD files from (old) PCAD to (new) Altium. Existing ECO will take highest priority over any new design feature! There was a brief discussion to consider the inclusion of a high speed Gigabit serial link to the CPU slot (PP-17), but there is not a great deal of time before the production lot must be ordered for the Hall D needs.

→During the discussion of the SD acceptance testing, it is clear that we can use the same idea for the acceptance testing of the CTP production units. In other words, use 16 fully tested FADC250 boards for the critical testing of the CTP production units.

### **16 March 2012**

Still a few bugs with the transfer of PCAD files to Altium. Merging power nets seem to not work properly.

ECO list is complete and new options are strongly considered and will be designed. E.g. PPT17 (Cpu slot) can run PCIExpress.

### **9 March 2012**

Files have been transferred to Altium. Problems! Need to get the Altium experts involved. Start ECO and set a schedule to get the board to production by July.

Plug but no play. A few issues with trying to run new HPS FADC250 and CTP code. Alignment testing and then cluster finding!

HPS group has sent simulation data to Ben. Ben is working on integrating this data into a full simulation of the FADC250 → CTP → SSP.

## **7. [GTP and Global Crate Developments](#)**

### **23-March-2012**

→HPS cluster finding code for the CTP has a few issues to work through. No show stoppers, meets timing, firmware changes, progress is still moving forward, ISE 13.2.

→Testing the dedicated cable link outputs with the TS prototype will need to be completed soon, but take a lower priority than the HPS activities.

### **16 March 2012**

→Scott has made significant progress with the HPS cluster finding firmware development and at some point soon all the components, (FADC250, TI, SD, CTPs and SSP) will have to be operated together. Hardware testing has started using simulation files to generate the input signals that will verify the new firmware (code). The schedule is still aggressive and by April the hardware will need to be assembled in Hall B.

**ACTION ITEMS: Next meeting -Friday 20 April@ 10AM in F226**