12GeV Trigger meeting notes:

21-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, B. Moffit

14-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, J. Wilson, B. Moffit

7-Sept-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, E. Jastrzembski

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0. Trigger/Clock/Sync – TI/TD

21-Sept-2012
→Acceptance approval memo has been delivered to the CEM and procurement.
→Rework/repair of the bad board should be complete next week. CEM sales rep will return the board.
→V1290 TDC fan-out board supports eight boards. More are needed for both Hall B and Hall D.
→Ask the Hall C and A groups about their requirements for the V1290 TDCs.
→Final delivery for the TI-D procurement is listed for Feb-2013
→Production firmware is ongoing. New CODA library will need to be update.

14-Sept-2012
→Production acceptance approval is due next Monday 17-Sept. The one bad board has been given to the sales rep, and the part will be x-rayed.
→14 of 15 boards are undergoing tests, no issues recorded.
→Trigger Supervisor testing: The TS Fpga uses GTX transceivers which will need adjustment in firmware.
→V1290 TDC fan-out board is complete. This fan-out board supports 8 TDCs.

7-Sept-2012
→Testing is progressing nicely. 1 of 15 boards has a power supply issue with the -5v.
→TS work is not the highest priority, and a CODA library exists
→Multiple crates in the DAQ lab to test the configuration and fiber drivers between TI and TD boards including an SD module.
→After acceptance test report is completed, CEM has 20 weeks to deliver the balance.

1. *SUB-SYSTEM PROCESSOR (SSP)*

21-Sept-2012
→Letter of increase to support extra layer requirement for production SSP boards and PRs for front panels will need to be approved. Use same POAs for front panel and miscellaneous hardware requisitions.

14-Sept-2012
→Parts will be received at Zentech on 17-October. Gerber files and other manufacturing data are due soon.

7-Sept-2012
→Zentech is proceeding with the BOM purchase. Some long lead times, so final route files not due for about a month.

31-Aug-2012
→1st article delivery is based on long lead components plus PCB fabrication.
→PCB fab/assembly files are progressing but will take a few more weeks for final review.

→Hall A requested an additional SSP and the PR was submitted and approved

2. CUSTOMERS

21-Sept-2012
→New topic for the Hall D BCAL trigger scheme. Presently just an idea, but as always, the development of new firmware will have to be considered.
→Initial beam running will be low luminosity, so the trigger will be derived from the tagger hodoscope and microscope.
→Hall D collaboration on 4-6, October and Hall B Collaboration the following week would be good opportunities to discuss other interesting trigger topics.

31-Aug-2012
→The Pre-Production batch of FADC250 boards has certainly been used extensively for testing and of course for HPS and other beam tests.
→No details on the PCAL group's request and we will have to shuffle boards around because there are other essential tests that are ongoing that require a full crate of FADC250 boards.

3. "B" Switch - Signal Distribution Module (SD)

21-Sept-2012
→CTP#4 was located in EEL109 and is loaded with the SD-test firmware.
→113 boards have been received with two remaining at the factory.
→25 of 115 have passed acceptance testing
→Full steam ahead on testing in the full crate and so far no assembly issues have been discovered.

14-Sept-2012
-->Need a CTP. Need to check where the #3 board is located so Nick can continue testing.
→Received 30 production boards.
→25 of 115 boards have passed acceptance testing.

7-Sept-2012
-->49 production boards have been delivered
→Remaining 55 boards will be here soon.
→SD test station is ready to go.

4. System Diagrams/Fiber Optics

21-Sept-2012
→FO patch panels and other hardware have been received for the Hall C trigger fiber installation.
-->Fiber trunk cable for the Hall C order can be tested with new Fluke meter and also in the EEL109 lab using trigger modules in the Global Test setup.

14-Sept-2012
-->Review FO diagram with Brad. Prepare for installation.

31-Aug-2012
→Fluke fiber test equipment has been delivered to Scott.
→Expect Hall C fiber to arrive in about a month
→Need to finalize the specification and quantities for trunk, patch, and patch panels, for the Hall B and Hall D order. Order in last part of 2013 first quarter. (Dec-2012)

5. Global Trigger & Trigger Distribution Testing

21-Sept-2012
→TI communications established through I^2C to GTP
→Register map definitions created by Scott and drivers developed by Bryan
→Third VXS crate moved to EEL109 lab. This unit will be configured as the Global Crate with SSP->GTP. Will need SD and ROC plus TI. The Densi-Shield cable will reach the Trigger Distribution crate and interface with the TS on the rear transition panel without issue.

24-Aug-2012
→Time to get the hardware mounted in the rack:
--1st crate – Global – SSP (FADC250), GTP, SD, TI
--2nd TS, SD, TD
--Densi-shield cables. Use two cables for now (15 trigger bits + clock)

17-Aug-2012
→Scott continues to test the GTP using FADC250 boards as the data generators. VXS Gigabit serial links are running @5Gb/s with a few errors, but long term data is needed to increase our confidence level to operate at the higher bit rates.
→No VME backplane readout is exercised during the serial tests, and 2eSST readout should be exercised during the 5Gb/s serial data transmission testing to replicate a real system test. What should the duration of the testing?

10-Aug-2012
→16 FADC250s used as data generators to GTP @5Gb/s with some errors, but over a 48 hour period. Good news. No equalization parameter adjustments yet, but this could be tested and documented.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)

3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

21-Sept-2012
→Jeff is very busy, and the schematic changes and net swapping list is progressing.
→Final BOM is important and needs to be ready to send as soon as the award is final (2wk of Oct?)
→16 layer circuit board is the goal, or additional funding requests will need to be generated.
→VHDL firmware for the acceptance testing of the production CTP is at 60%. This will take a lower priority because the production FADC250 test procedure program needs modification.

14-Sept-2012
→Evaluate low bid paperwork. Need a decision by Monday 17-Sept-2012
→Continuing on the layout, a few schematics need to be corrected and then the full routing plan will ensue. BOM needs to be updated.
→CTP acceptance test development is in progress.

7-Sept-2012
→CTP automated test is 50% complete
→Production TI will be ready for Hai in two weeks.
→Jeff is on vacation, routing the CTP is on hold.
→Bids are due 7-Sept. Lowest price wins.

31-Aug-2012
→1 CTP added to the PR for the Hall A group.
→Bid packages due after Labor Day.
→Placement is in progress, and then will progress to optimizing the routing file.
→Development of the CTP acceptance test program is progressing.

GTP and Global Crate Developments

21-Sept-2012
→SSP firmware is in rework to be used for the global (GTP) testing.
→Move a (Hall B) VXS crate to EEL-109 for dedicated testing of the global hardware.
→Beg, borrow, and steal CPU, SD, and TI, to keep in EEL109 until hardware testing is complete for the global hardware.

14-Sept-2012
-->Turnkey order for single GTP has been approved.

7-Sept-2012
See Scotts presentation

31-Aug-2012
-->Consolidation of separate firmware projects is progressing.
→Register map under implementation. More definitions and driver development will occur.
→Keep progressing toward goal of the Global Crate test. Several minor details still to complete but getting closer to the goal!

24-Aug-2012
→2.5 days running @5Gb/s with 16 FADC250 boards without errors recorded.
→The serial tests are performed without VME bus activity
→Serial testing should be performed with VME bus activity
→Embedded controller on the Altera part to manage serial testing? Sidetrack,
→GTP driver development started. i.e.(I^2C control, etc)
→Final Physics equation loading? Are we going to use Playback mode?

***ACTION ITEMS*: Next meeting - Friday 28 September @ 10AM in F226**