Trigger meeting notes:

30 Jan 09: C. Cuevas, A. Gupta, H. Dong, E. Jastrzembski, B. Raydo, J. Wilson, M. Taylor

23 Jan 09: C. Cuevas, A. Gupta, H. Dong, E. Jastrzembski, F. Barbosa, J. Wilson, M. Taylor

16 Jan 09: B. Raydo, C. Cuevas, A. Gupta, H. Dong, A. Somov, E. Jastrzembski

Updated prototype board status table:--23 Jan 2009

Quantity	Description	Location	STATUS
7	10bit FADC250	EEL109/DAQ Lab	Trigger testing
1	10bit FADC250	EEL109	In Repair
1	12bit FADC250	Indiana University	FCAL testing
4	Trigger Interface Trigger Distribution	EEL109/DAQ Lab	Trigger testing
5	VME -- FP-SD Front Panel – Signal Distribution	EEL109/DAQ Lab	Complete Use in test crates
1	Crate Trigger Processor	EEL 109	Initial functional testing
1	Crate Trigger Processor	Send for assembly as soon as parts received	Send 9 Feb 2009
2	Signal Distribution	Receive from board house on 21 Jan	Ship to assembler on 29Jan09

0. Trigger/Clock/Sync – TI/TD

30 Jan 2008

Sebouh will move his application to the EEL109 lab and test his firmware and GUI for the I^2C read/write functions to the CTP and SD. He is using MSVisual Studio for the GUI and is preparing the lab PC with the proper files, etc for testing his application. He will use the Wiener USB-VME controller to execute VME commands to the Trigger Interface.

23 Jan 2008

No report and the TI modules are functioning without problems and the latest firmware has been stable since installation about a month ago.

Sebouh has returned to school and is at a point where he can demonstrate his work on the GUI and interface code that will be used to control the Signal Distribution card and the CTP card. His application will read/write data to the Trigger_Interface module with the Wiener USB-VME controller. His I^2C firmware will be used on the Atmel microcontroller which bridges the information from VME to the two I^2C devices. (SD and CTP).

1. FIRMWARE TESTING

30 JAN 2009

Ben has identified a firmware bug when attempting 64bit bus transfers. Ed acknowledges the problem and troubleshooting has started on the TI and FADC250 modules.
→Work on the VME – SST firmware development and testing will take a higher priority after the 64 bit data transfer 'bug' is understood.

23 JAN 2009

→The firmware for the FADC250 modules has been stable for many months, including the updates to the TI module.

→We discussed the effort required to develop and test the Source Synchronous Transfer (SST) mode to achieve higher VME data transfer rates. Ed described the two edge VME transfer mode and associated handshaking requirements, and explained that it makes more sense to put full development effort into the SST method because the readout controllers(ROC) support this SST method. This development effort will take a higher priority because we need to test the data readout rates in combination with the specified 200 KHz trigger rate.

→Hai explained that the present firmware will sustain 165 KHz trigger rate using the "Q" readout mode. Optimization of the firmware will develop as soon as we begin the production design.

16 JAN 2009

No problems to report and the new readout parameters have been added to Ben's test stand data displays and records.

Hai has completed the development of the firmware download procedure that describes the method to reconfigure and download the FADC250 FPGA from VME. The discussion that followed focused on the method to verify that the new firmware download was successful. This download procedure will be refined, and the main point is that Hai has developed the code that manages the transfer of the new firmware via VME to the Xilinx Eproms.

2. *Sub-System Processor (SSP)*

30 JAN 2009

For the alert readers, this section has been changed to the SSP activity notes. Chris has transferred the Pcad files for the TI into the Altium "Unified" application and modification to the schematic sheets is a work in progress. The SSP is a VXS payload module, so it makes sense to re-use all of the board components and circuitry that will be used for the SSP. Ben has suggested new Virtex5 series components for the initial board, and I am certain several parts will have to be created with the Altium tools for the SSP design. We will have to revisit the proposed design for the global trigger crate and sort out the details as we continue the schematics.

3. CUSTOMERS

30 JAN 2009

→Ben presented recent measurements of the FADC pulse sum mode, and SNR testing with a 10 bit module at the GlueX collaboration. I talked with Matt Shepard from IU and he thought it was a good idea to run the SNR testing on the 12 bit FADC module so that we can measure and compare to the 10 bit version. The final version of the FADC250 module will include 12bit parts, so it will be a good test, and we should only need the 12 bit board for a few weeks.

→I have decided to loan a single FADC250 module to the instrumentation group at ORNL for a short period, so that they can run an evaluation/demonstration of the board. The ORNL group has significant upgrade projects for several beamline systems and one of their proposals is a very expensive COTS solution. Our FADC250 design may prove much more cost effective for their application, and since we are both DOE labs, it makes sense to share this type of design and possibly combine funding.

23 JAN 2009

→Collaboration meeting for GlueX starting 29 Jan and it would be a good opportunity to discuss details of the results from the FCAL group at IU. Schedule priority is still focused on the CTP testing, but code development plans for implementing the algorithm in the FPGA for the timing readout can begin.

→There is a group at Oak Ridge National Lab that has an interest in implementing the FADC250 design for their Accelerator upgrade projects. Since ORNL is a DOE lab it should be

easy to exchange the design with them, and to request funding from them when we are prepared with the next revision of the board for production quantities.

16 JAN 2009

No new progress to report. Hai has focused his time on the CTP testing.

Alex Somov had a few questions about the ability to readout raw data AND 'Q' value from each channel for every trigger event. This may be a method used during commissioning to verify the 'Q' mode function that is performed in the Fpga. Other system level trigger questions were discussed and it is clear that further discussion is needed to document/clarify overall trigger system requirements/functions.

4 "B" Switch - Signal Distribution Module (SD)

30 JAN 2009

→The bare boards were tested and two voltage 'polygons' on the power planes will have to be connected together externally with jumper wires. There are zero power to ground connections and the boards have been sent to the assembly house in California along with all the components. Expected delivery should be the week of 9 Feb. Abhishek and Mark will begin DC testing and other initial measurements as soon as the boards are received.
→The front panel design is close to complete and will need to be sent for machining soon.
→Abhishek has completed the firmware that will be used to initially test the functions of the SD. Further firmware development and testing will be generated as required to test ALL functions of the SD in the 20 slot VXS crate.

23 JAN 2009

The three bare boards have been received and look fine. Abhishek and Mark will begin testing the bard board for any defects and send these boards with the parts to the assembler. Schedule to ship on 29Jan09 and we paid for a seven day delivery.

As soon as the assembled SD boards are received there are plenty of preliminary functional tests to perform and these test results will be documented on Abhishek's test plan. Soon after, the SD will be installed in the full 20 slot crate and critical testing of the signal fan-out will begin.

16 JAN 2009

Abhishek presented his latest Altera functional timing verification for the FPGA that will control the Clock, Trigger, Sync, Busy and Token passing signals. He has successfully synthesized the firmware, and has instantiated the block of code that was developed by Sebouh Paul that will manage the serial control interface to/from the Trigger Interface module.

The SD boards will be shipped on 21 January, and two boards will be sent to the assembly company by next week (26Jan09). The assembly process is at least a week, and then Abhishek can begin the initial test plan for the SD board. Soon after, the SD board will be used to distribute signals in a full VXS crate and plenty of other tests can be performed.

There was a discussion about how to handle "half" crates that may be installed on experiments. In a 12 slot VXS crate, the payload slot that would normally have the Trigger Interface module does not exist.(PP18) This means that the SD and CTP would have to receive the global clock/sync/trigger signals from a front panel module. For Hall D, I believe we have specified full 20 slot VXS crates for all the detector readout systems, so this should not be an issue.

In cases where a VXS "half" crate is used, the CTP will have to receive the common signals (CLK,Trigger,Sync) from the front panel. This detail will have to be discussed further and implemented on the final board design.

5. System Diagrams & Test Stand Activities

30 JAN 2009

Ben presented results at the GlueX collaboration meeting, and no other report was given at the Trigger meeting. Notes from previous meetings are included below, and there will be many more tests to perform when the CTP and SD are completely tested.

23 JAN 2009

→No report since Ben was out this week. Results from recent measurements in the test stand will be presented at the Hall D Collaboration meeting.

→Many more tests are planned once the CTP and SD boards are ready to be installed in the test stand crates.

→A new RF switch has been purchased and will be controlled with a FlexIO module. This switch will allow us to connect each input on the FADC250 module to a single signal source. The present pulse source is an Agilent arbitrary waveform generator, but in principle, the signal source could be a PMT.

→The Wiener 21 slot VXS backplane will be installed in one of the test stand crates on 4 Feb 2009. The other crate will retain the Elma 20 slot VXS backplane and we can verify that the new Wiener design meets specifications.

16 JAN 2009

As a quick review, the following tests have been completed with the FADC250 boards, TI/TD, and front panel signal distribution boards:

- ✓ Test LX25 with high rate trigger pulse train on all inputs simultaneously
- ✓ "System" clock jitter with fiber distribution and existing front panel signal distribution boards. These tests will need to be repeated once the SD module is ready.
- ✓ Signal to Noise Ratio (SNR) Plenty of test data, and the results so far will establish the baseline SNR value. These tests should be performed with multiple channels per board, and with multiple boards transferring VME data and with all the Gigabit links active to measure differences from the baseline results. VME data transfers are not dual edge yet, but testing SNR with higher the higher bus rates will be important
- ✓ 10 bit FADC250 charge mode Vs 12 bit charge integrating ADC(LeCroy 1182) Ben presented the initial results from the test, and further details will be presented at the Hall D collaboration meeting.

GUI and data display software will continue to be developed by Ben for the upcoming CTP and SD test stand activities.

- Real Time Conference 2009 – Beijing, China 10-15 May, 2009
  Dave Abbott proposed that abstracts be created for submission and that the 12GeV trigger system offers an abundant source of topics to present at the conference. The overall Trigger/DAQ system could be the main presentation, and the poster sessions could present details of new results from the CTP and SD crate tests. Abstract submission deadline is 20Feb2009

6. Crate Trigger Processor (CTP)

30 JAN 2009

→Successful GTP testing has been accomplished in the test crate with a single FADC250!
→Heat sink material will have to be machined and mounted to the CTP so that adequate cooling is provided as more GTP lanes are activated.
→Hai briefly described the goal of the two crate configuration for testing the CTP, SD and two FADC250 per VXS crate. This configuration will be described in the poster/paper for the Real Time Conference. This will be the first time for testing the Gigabit Transceivers with FADC250 boards in PP15 and PP16, and with the SD boards driving the clocks, trigger and sync signals.

23 JAN 2009

Loopback testing is underway for the initial CTP module. The heat sink material has been ordered and the material will need to be machined to fit properly on the CTP board. The heat sink will cover all three FPGA will provide adequate cooling for the Virtex5 parts when the full code is running all SerDes lanes. We cannot activate all 16 payload slots, but we can certainly test the CTP with up to 8 FADC250 modules.

16 JAN 2009

Functional testing with the first module is going well. A heat sink will be added to cover the three large Fpga on the module. Hai will follow his test plan for the initial functional testing and then begin the testing with multiple FADC250 modules in a crate. Discussions about how to use the CTP output data were presented, and since we will not have a SSP module for awhile, we could implement the testing of the CTP fiber optic output data stream with a Xilinx evaluation board. We may not be able to fully implement the 4 lanes of fiber optic data, but the final CTP sum data can be tested.

ACTION ITEMS: Next meeting will be Friday 6 February 2009 → CCF228 @10am