Trigger meeting notes:

1May 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, J. Wilson

24 April 09: No meeting

17 April 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, J. Wilson, D. Abbott

10 April 09: No meeting

Updated prototype board status table:--22 May 2009

Quantity	Description	Location	STATUS
5	**10bit FADC250**	**EEL109/DAQ Lab**	**All boards are in use.. Source Synchronous Transfer (SST) Firmware in final test**
1	**10bit FADC250**	**EEL109**	**Received from ORNL**
1	**10bit FADC250**	**EEL109/DAQ Lab**	**Experiment testing successful! Returned to DAQ Lab**
1	**10bit FADC250**	**EEL109**	**Needs repair; Clock Issues**
1	**12bit FADC250**	**EEL109**	**Returned to IU May09 SNR tests complete Ben**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** Front Panel – Signal Distribution	**EEL109/DAQ Lab**	**Complete Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Fixed pin mode works. Programmable features still being tested. Token passing mask and busty mask need to be verified before using with FADC250 modules.**

0. Trigger/Clock/Sync – TI/TD

1May 09

Sebough has completed the Virtex 5 voltage and temperature monitoring code for the CTP. I do not know if this information is displayed on the CTP GUI but we can ask for a demonstration soon.

17 April 2009

C code from Sebouh is used when using the Motorola SBC to interface to the TI and CTP. Ben has slightly modified the code but progress continues. The present design of the TI relies on a microcontroller from Atmel to manage the I^2C data from the switch slots. (CTP and SD respectively).

CTP readback is complete, and Ben is integrating the control code with his MSVisual Studio and Root GUI.

SD board is ready to test with control registers by close of business today, 17April09. Abhishek has been working on the Altera code for controlling the required registers on the SD

board. These control registers are not required for the two crate test, but will need to be thoroughly tested to complete the prototype design phase.

1. FIRMWARE TESTING

1MAY09

Hai has a new firmware breakthrough for the LX25 code and the improvement changes are specific to the output fifo stage. Simulations show factor of six improvement and a board has been tested with a few channels operating at trigger rates to 310KHz!!! This definitely exceeds the design requirements and more testing will be needed to verify this operation with multiple FADC250 in multiple crates.

The Altera interface needs to be changed to interface the new requirements for the Moller application. Ed will need to alter this firmware.

17 April 2009

Significant progress has been completed with the VME-SST firmware. Several (4) FADC250 boards have been loaded with the new SST firmware and testing continues in the lab. Token passing with multiple boards has been tested, and the token passing scheme appears to work. We can use wire jumpers on the backplane (P2) to test the boards in the two crates in case the SD board token passing logic is not ready.

2. *SUB-SYSTEM PROCESSOR (SSP)*

1 May 09:

No significant progress has been accomplished. Ben was able to point out a few corrections to errors because of the hierarchy mode, and Chris will continue at the glacier pace to complete the schematic.

17 April 2009

Altium CAD files presented and the FPGA have been added to the schematic successfully. The hierarchy tools for the front end fiber optic receiver circuits has been used, and there are several errors to correct before all of the components are correctly loaded in the circuit board 'project'. Many schematic circuits need to be defined yet, but progress is detectable.

3. CUSTOMERS

1 May 2009

→The 12 bit 8 channel FADC250 has been thoroughly checked and Ben managed to set up a test to show an FFT plot with and without the SST bus activity. The short story is that the SST bus transfer does not appear to disrupt the channels that are measuring input signals. The additive bus noise is almost immeasurable, but it does show up on the FFT but at a point which is less than a LSB.

→Hall A Moller FX20 trigger logic is complete. Changes to the LX25 FPGA are almost complete. We can setup a test for the input using the 16 channel fanout board soon. I believe that there will be a few modifications required from Ed for the Altera device to control the trigger logic that will be implemented on the FX20.

17 April 2009

→Hall A has presented a proposal to use a prototype FADC250 module for their Moller experiment scheduled for September '09. Hai has completed the firmware and has simulated the code. Ed will need to add the new features for the Altera FPGA and a few software 'library'

changes need to be added to control these new features. Testing the new firmware for the Moller application will be a lower priority than the two crate trigger testing.
→Brad Sawatsky presented data that was collected by an FADC250 prototype module on a recent Hall A experiment (Big Bite Cernkov detector). The results were encouraging and he seemed pleased with the results. There was a question about optimizing the 'window' and look back time, but they were able to write the necessary analysis programs to use the data.
→The eight channel 12bit module will be sent back to the IU-FCAL group before the end of April. Ben has collected SNR data and if there is time, it would be nice to run a test to compare the 12bit FADC250 to the LeCroy QDC module. Ben has recorded the results from the comparison of the 10bit FADC250 Vs the LeCroy QDC, so the results from the 12 bit module would be interesting.

4 "B" Switch - Signal Distribution Module (SD)

1 May 2009
→The SD boards are working well in the test stand and these boards have 'fixed' pins in the code. The clock selected is 250MHz for both even and odd payload ports. The control registers are still under functional testing and Abhishek has made some progress with the token passing mask scheme. The control registers are being controlled with Sebouh's GUI to read and write the proper bits to select and monitor the clock lines, and also set the mask registers for the token passing and busy signals. The mask register will have to be loaded manually to bypass the signals from the missing payload port slots. The internal logic on the SD board will properly pass the token signal to the slots that contain Payload modules.
Block diagrams of the token pass test plus logic diagrams for setting the busy mask register should be distributed at the next meeting for discussion.

→The schematics and circuit board should be transferred to Altium as soon as possible. Verify that the parts library is intact and begin the ECOs for the final revision. We should review what components need to be eliminated or enhanced. The switch settings for the fine delays may be able to be removed, and we should also look at using a CML fanout so that the pECL pull down and termination scheme can be simplified.

17 April 2009
→Abhishek presented waveform photos from the oscilloscope for a variety of payload ports and signals. The clock waveforms and pulse shapes for the SYNC and TRIG signals appear to be the correct levels and there were a few pulse shapes that did not look consistent. The scales on the O'scope need to be the same, and some of the pulse shape attributes, (i.e. risetime, fall time) were attributed to the high speed differential O'scope probe connections. Good news is the signals appear without excessive ringing, or other anomalies.
→The control code for the SD Altera device is progressing. Controlling the select lines to choose which payload slots receive a specific clock, and writing the mask register for the BUSY and TOKEN IN/OUT signals will need to be verified with Sebouh's I^2C firmware. Implementation and functional testing continue.

We will continue to test with both VXS backplanes and record any differences. The PayloaPort mapping from Wiener is their creation and effectively makes the design a sole-source. Several companies sell 20 slot VXS backplanes using the 'Elma' port mapping, and we have designed the SD and TI boards to follow. The Wiener backplane is not unusable, but it adds a bit of confusion to an already crowded room full of slots, port maps, pins, lanes, switch slots, etc.

5. System Diagrams & Test Stand Activities

1 May 2009

LabView test stand has been revised! We have eliminated the 1990 MXI interface and Mark has updated the routines using LabView and the Wiener USB-VME bridge. We can put this to the test soon because the two crate test stand will not be in use once the SD full functional tests have been completed. This means that a FADC250 board can be dedicated to developing the LabView board testing software. Extensions to the LabView board tests could include the SD and CTP as stand-alone tests. Both of these tests will require a TI and USB/VME bridge.

17 April 2009

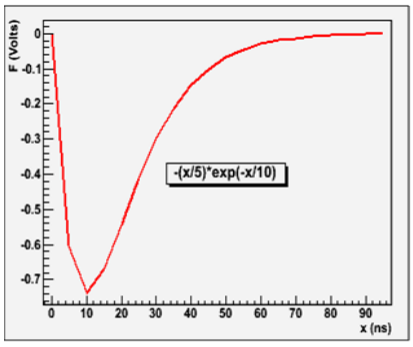
Nothing new to report, and other items have become a higher priority, but Jeff mentioned that the initial routing to a single FPGA for all sixteen ADC will work on four routing layers. The cost analysis of using a single FPGA will need to be performed for the Rev-1 design. Virtex 6 anybody?

6. Crate Trigger Processor (CTP)

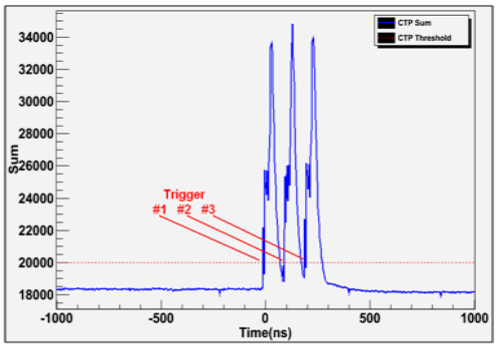
1May09

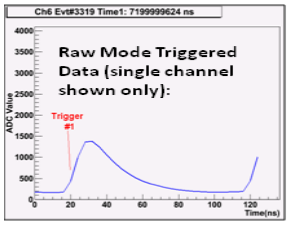
Two boards working successfully with two crates. One CTP functioning as a SSP and this works very well also. More testing can be performed with 6 ADC in one crate, but other projects will take priority. Need to update the rack photo to include CTP and SD. New photo updated in the IEEE-RT 2009 poster and SSP mode works fine. See results below:

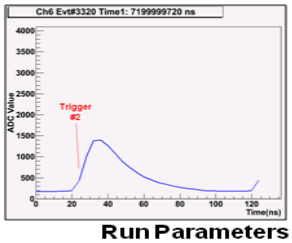
Input Signal(To 16 ADC Channels):

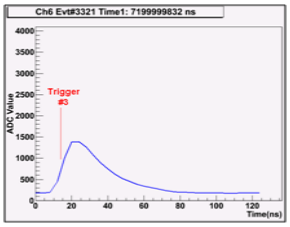


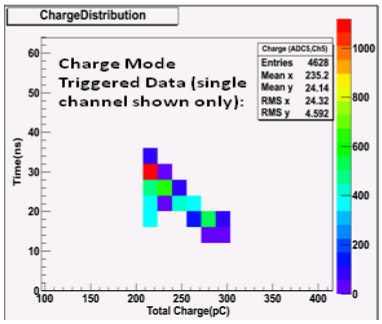
ADC Global Sum Capture:











Run Parameters:

Raw Mode: 120kHz trigger rate (140kHz max), 16 hit channels, ~110MB/sec

Charge Mode: 150kHz trigger rate (175kHz max), 16 hit channels, ~40MB/sec

FADC Window Width: 128ns (32 samples)

Input signal: 120-150kHz, burst of 3 pulses separated by 100ns @ ~40-50kHz

Digitized Sum: 2 crates, 6 FADC, 16 Active Channels

17 April 2009

Hai's test plan continues and the firmware that will be used to capture input pulses to the ADC will be installed and tested next week. The two crate test results are imminent and Hai has generated many hours of successful data transfer between the FADC modules and the CTP. All bit codes have been thoroughly tested, and the SD module has been used to clock and synchronize the boards in the system. The plan is to use four FADC in one crate, and two FADC in the second crate, all clocking from a single TI, synchronized and producing a trigger from a given set of input pulses.

ACTION ITEMS: **Next meeting will be Friday 29 May 2009 → CCF228 @10am**